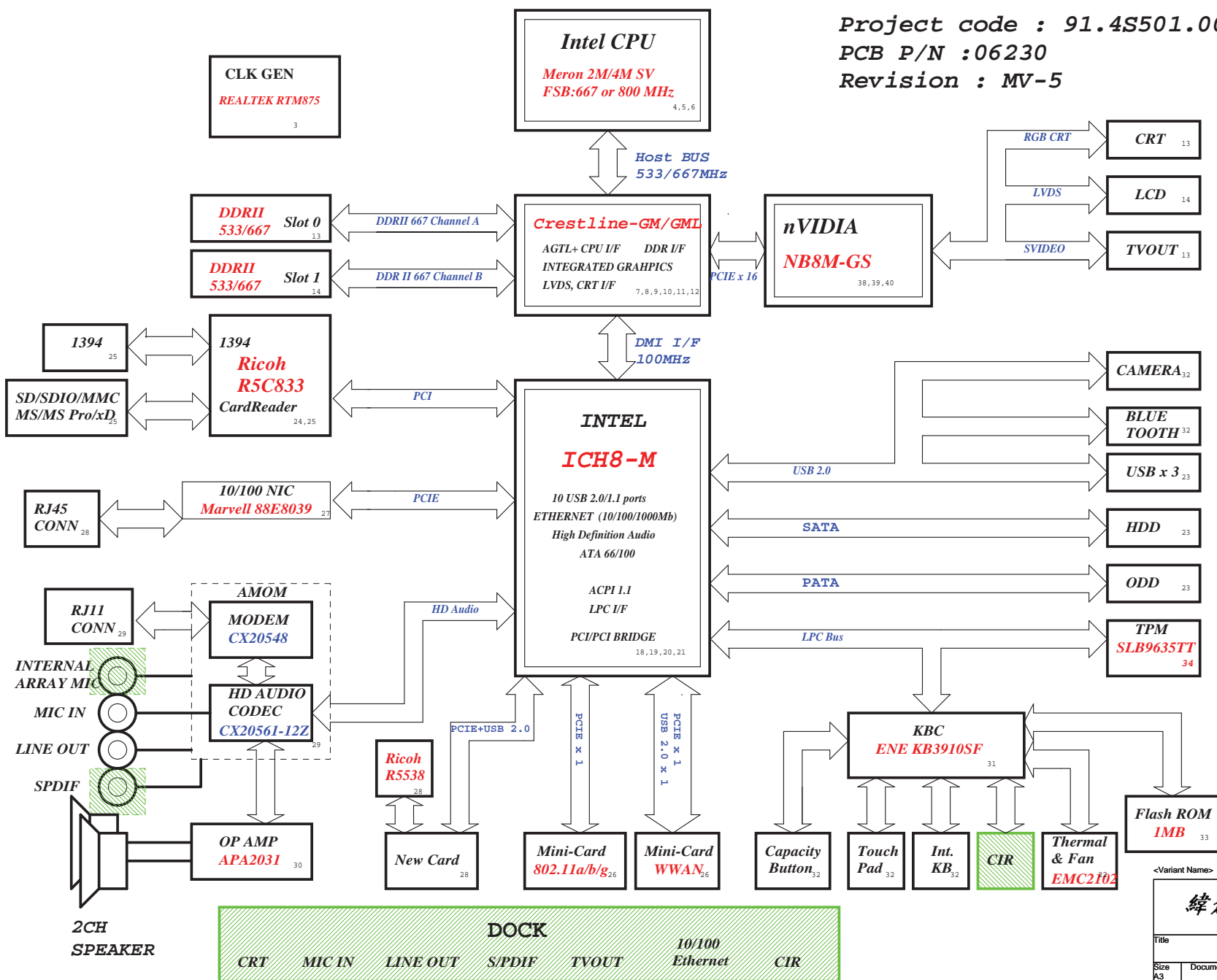


Viking-Discrete Block Diagram

Project code : 91.4S501.001
PCB P/N : 06230
Revision : MV-5



SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS
DCBATOUT	5V_S3 3V_S5

SYSTEM DC/DC MAX8743	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

SYSTEM DC/DC FAN5234	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0 11A

MAXIM CHARGER MAX8725	
INPUTS	OUTPUTS
DCBATOUT	BT+ 18V 3.0A 5V 100mA

CPU DC/DC MAX8736ETL	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 0.844~1.3V 44A

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 5

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Title: **Block Diagram**

Size: A3 Document Number: **Pamirs-Discrete** Rev: **-5**

Date: Wednesday, September 12, 2007 Sheet 1 of 47

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:Offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved	Weak Internal PULL-DOWN. NOTE: This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05, VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL. Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK	If sampled high, the system is strapped to the "No Reboot" mode (ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit. (Offset: 3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Internal Pull-Up. If sampled low, the Flash Descriptor Security will be overridden. If high, the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap			
ICH_RSVP#3	AZ DOUT ICH	Description	
0	0	RSVP	
0	1	Enter XOR Chain	
1	0	Normal Operation (default)	
1	1	Set PCIE port cofin bit1	

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable high = default	
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

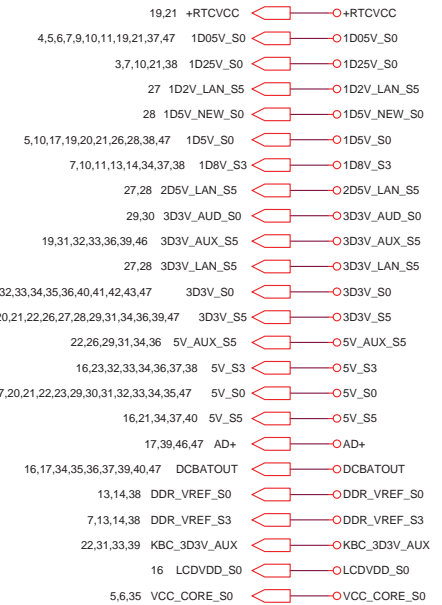
DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

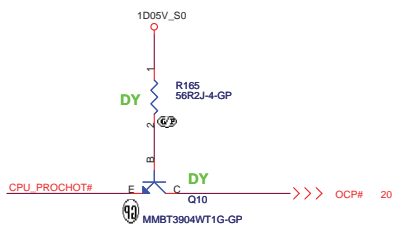
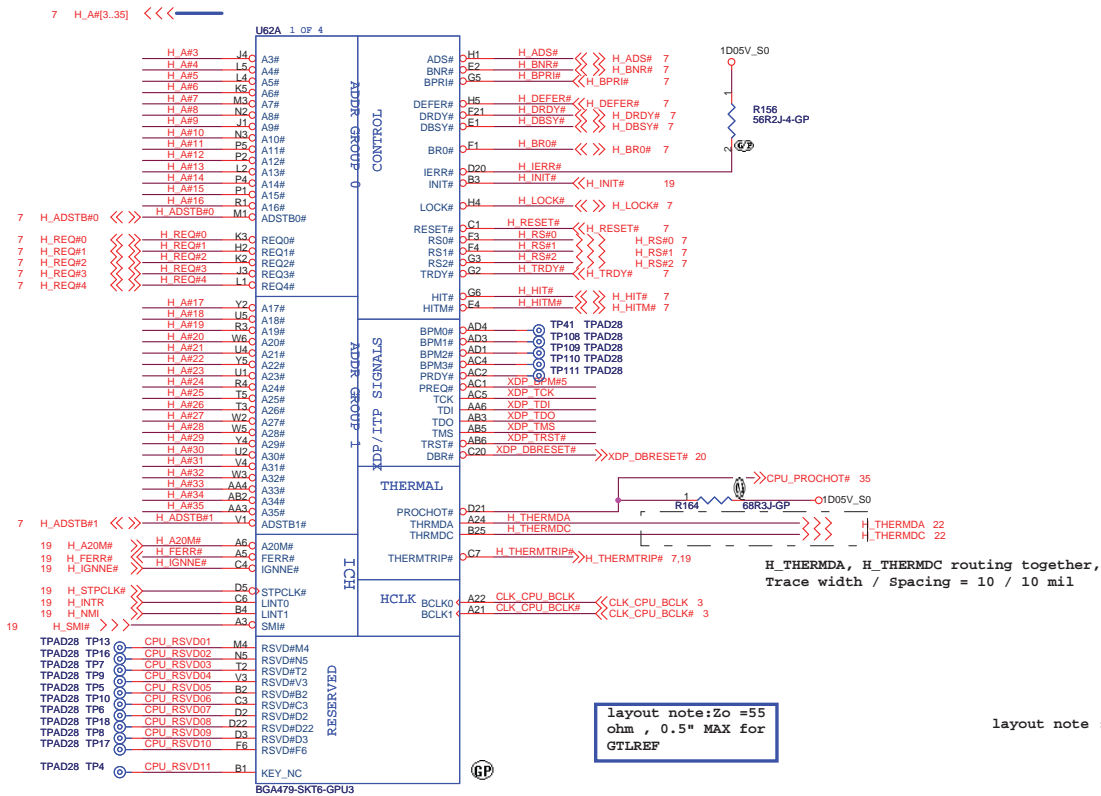
SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 20K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	TBD



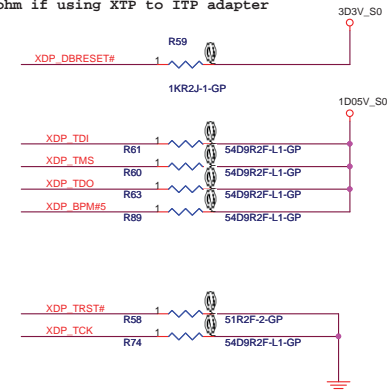
INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 8 Low Power PCI Express	Normal ★	Low Power mode
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode (Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present
CFG 12	XOR/ALL-Z	
CFG 13	Reserved	
LH(0)	Reserved	
LH(1)	XOR Mode Enabled	
HL(10)	All Z Mode Enabled	
HH(11)	Normal Operation	

<Core Design>		
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Title		
Table of Content		
Size A3	Document Number	Rev
	Pamirs-Discrete	SA
Date: Wednesday, September 12, 2007	Sheet 2 of	47



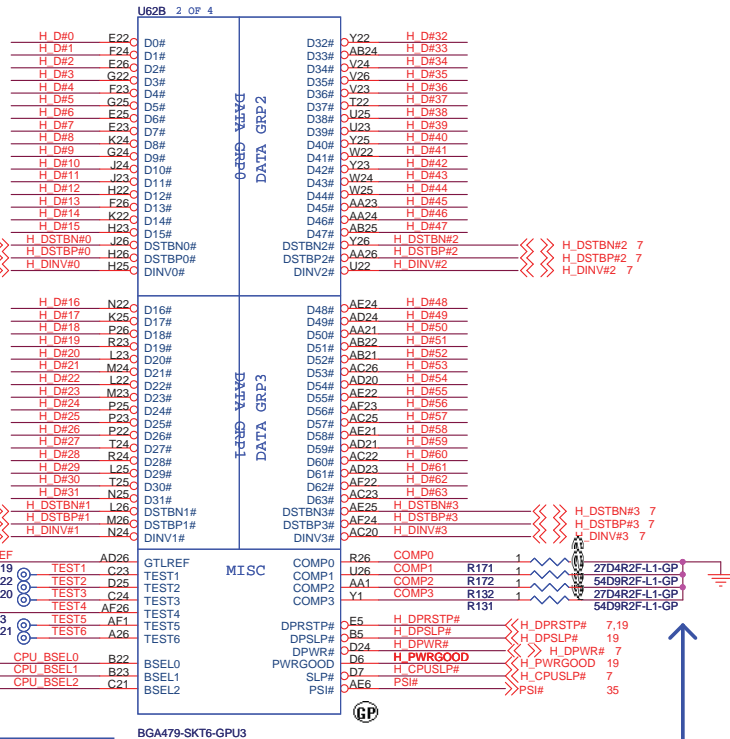
layout note : Change R237 to 649 ohm if using XTP to ITP adapter



<Core Design>

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Title			
Meron(1/3)-AGTL+XDP			
Size	Document Number	Rev	
Custom		SC	
Date:	Friday, September 14, 2007	Sheet	4 of 47

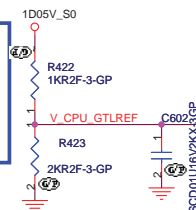
7 H_DW[0..63] << >>



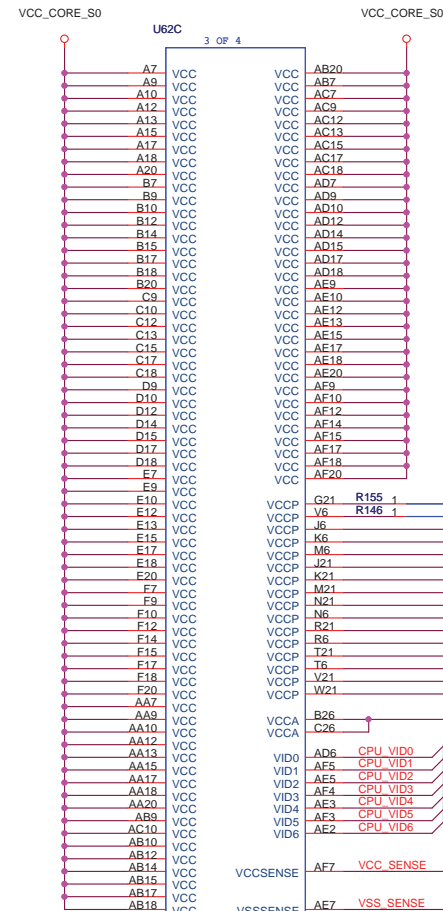
PLACE C173 close to the TEST4 PIN, make sure TEST3,TEST4,TEST5 trace routing is reference to GND and away other noisy signals

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

Close to CPU pin AD26 Z0=55 ohm with in 500mils .



Resistor Placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal . COMP[0,2] trace width is 18 mils. COMP[1,3] trace width is 4 mils .



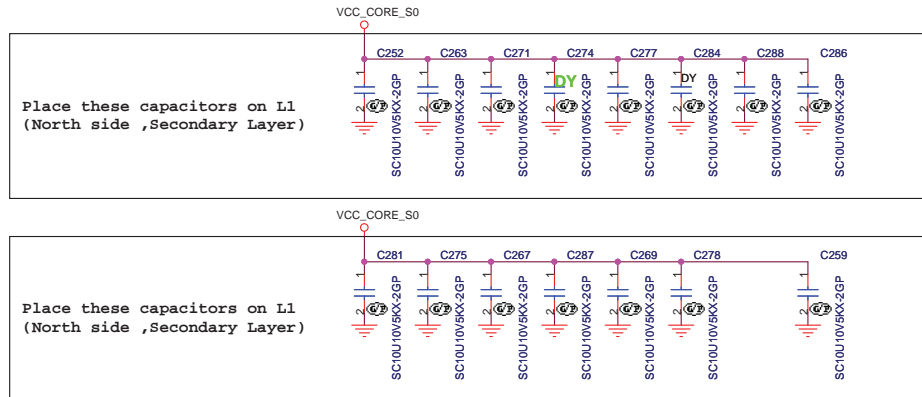
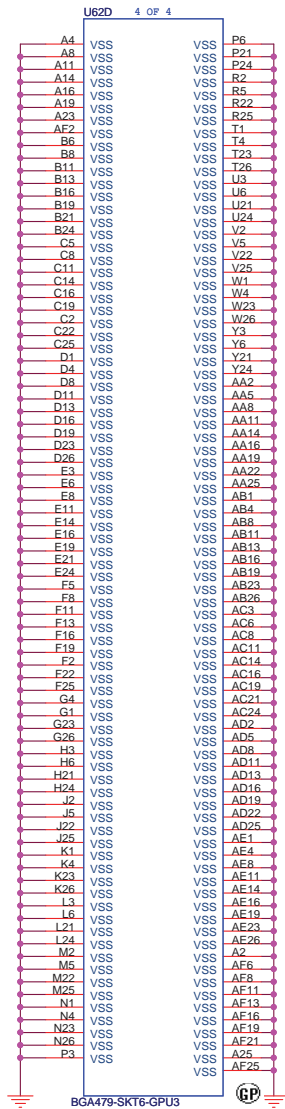
Close to CPU pin within 500mils

Length match within 25 mils . The trace width/space/other is 20/7/25 .

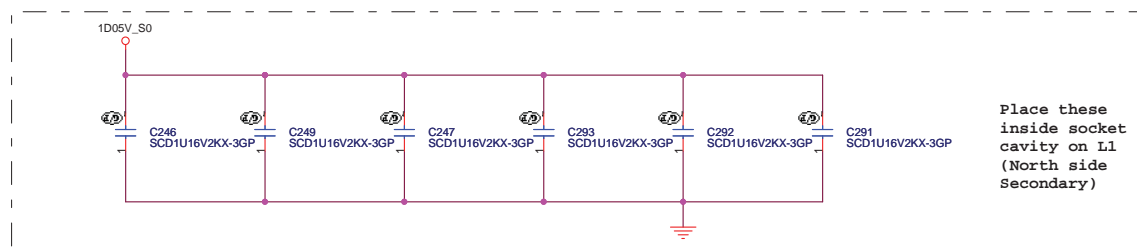
layout note: place C3 near PIN B26

<Core Design>

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Title Merion(2/3)-AGTL+/PWR	
Size A3	Document Number Pamirs-Discrete
Date: Wednesday, September 12, 2007	Sheet 5 of 47



Mid Frequncd Decoupling



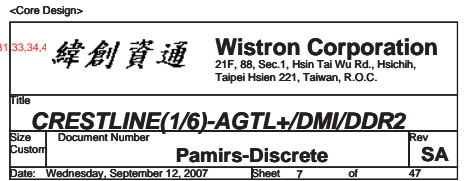
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Title: **Merom(3/3)-GND&Bypass**

Size: A3 Document Number: **Pamirs-Discrete** Rev: **SC**

Date: Wednesday, September 12, 2007 Sheet 6 of 47

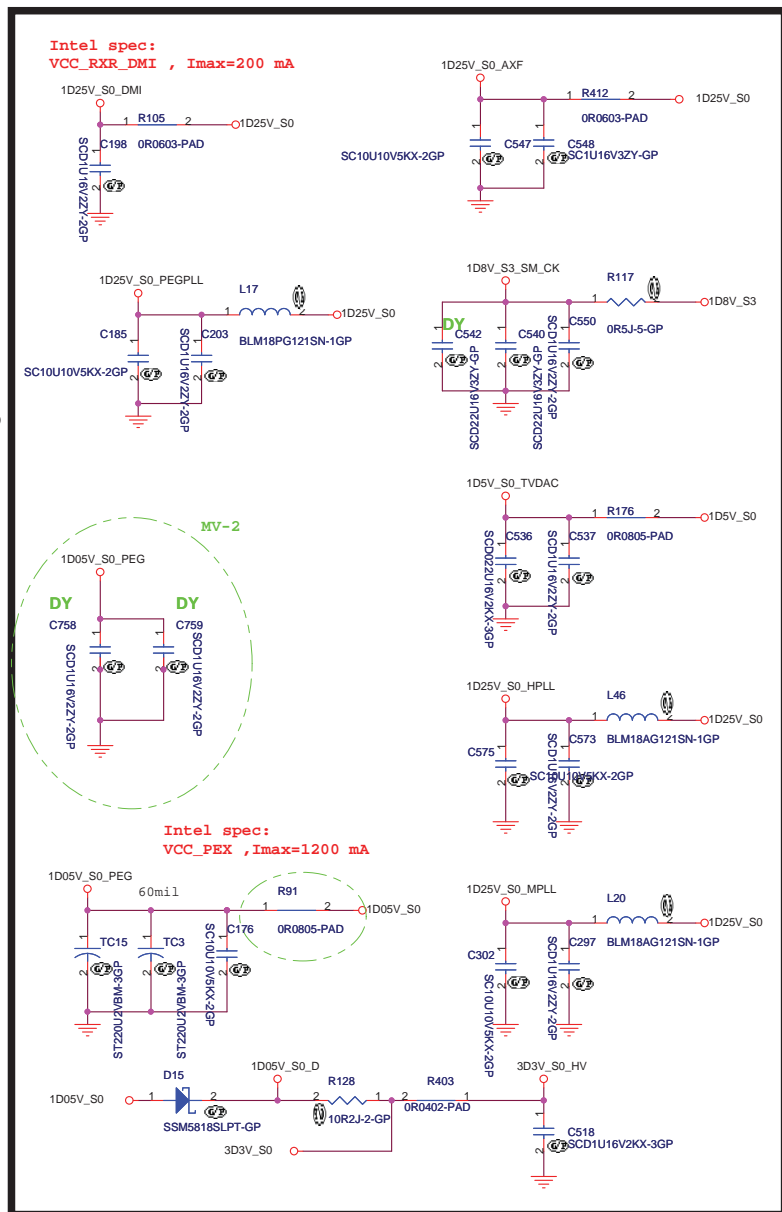
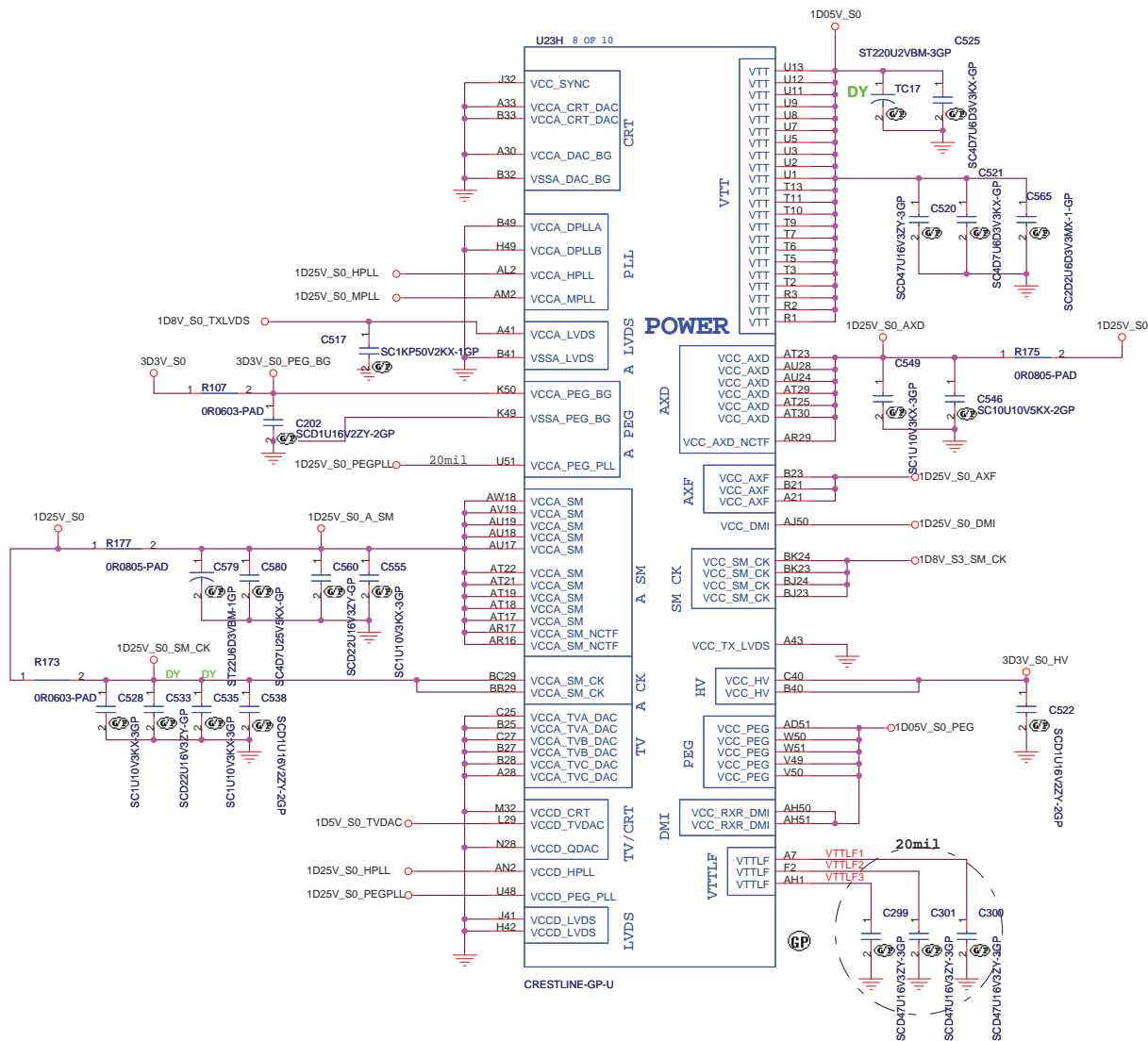






CFG[2:0] FSB Freq select	010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	Reserved
CFG7 (CPU Strap)	0 = Reserved 1 = Mobile CPU *
CFG8 (Low power PCIE)	0 = Normal mode 1 = Low Power mode *
CFG9 (PCIE Graphics Lane Reversal)	0 = Reverse Lane 1 = Normal Operation *
CFG[11:10]	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation (Default)*
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disable 1 = Enable *
CFG[18:17]	Reversed
SDVO_CTRLDATA	0 = No SDVO Device Present * 1 = SDVO Device Present
CFG19(DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse lane
CFG20(PCIE/SDVO concurrent)	0 = Only PCIE or SDVO is operational * 1 = PCIE/SDVO are operating simu.

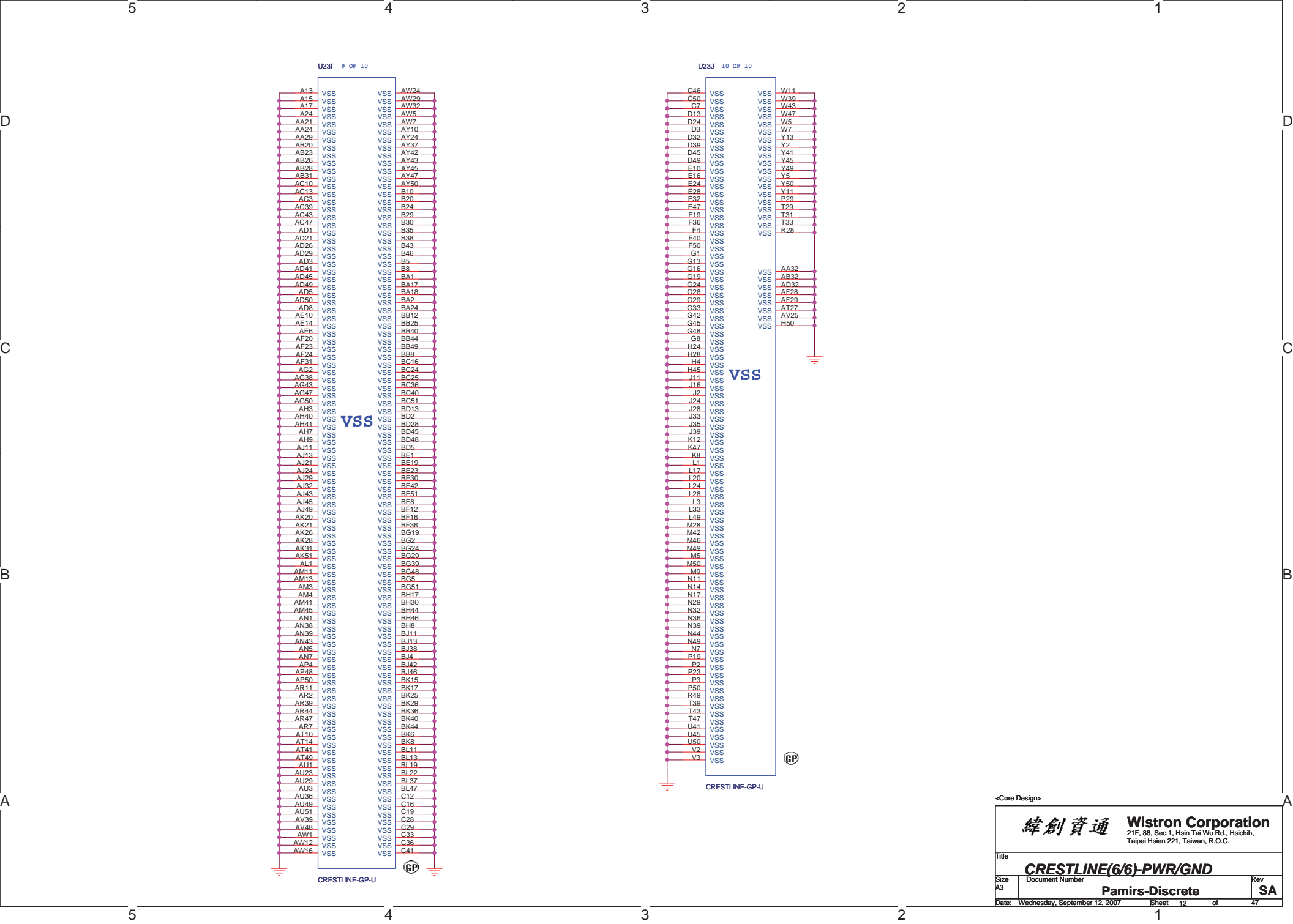
Date: Wednesday, September 12, 2007 Sheet: 3 of 47



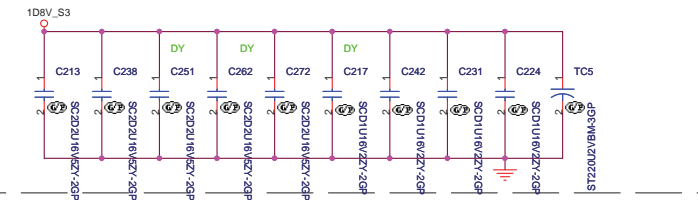
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Taipei Hsien 221, Taiwan, R.O.C.

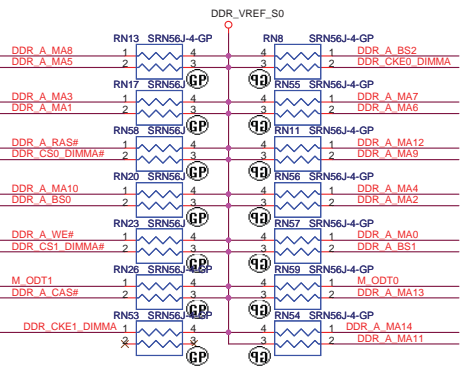
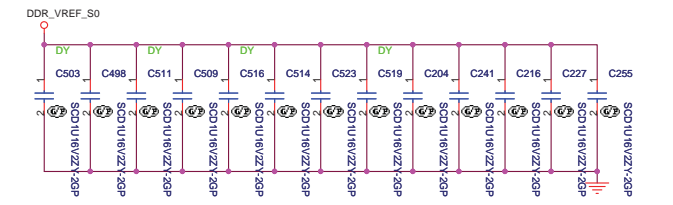
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Size A3	Document Number		Rev
	Pamirs-Discrete		SA
Date:	Wednesday, September 12, 2007	Sheet 10 of 47	



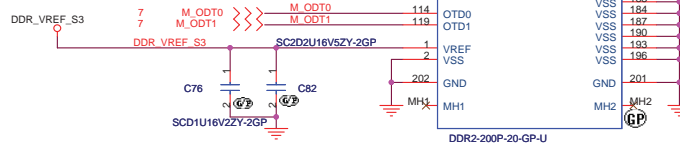
Layout Note:
Place near DM1



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistors
closely DM1,all
trace length Max=1.5"



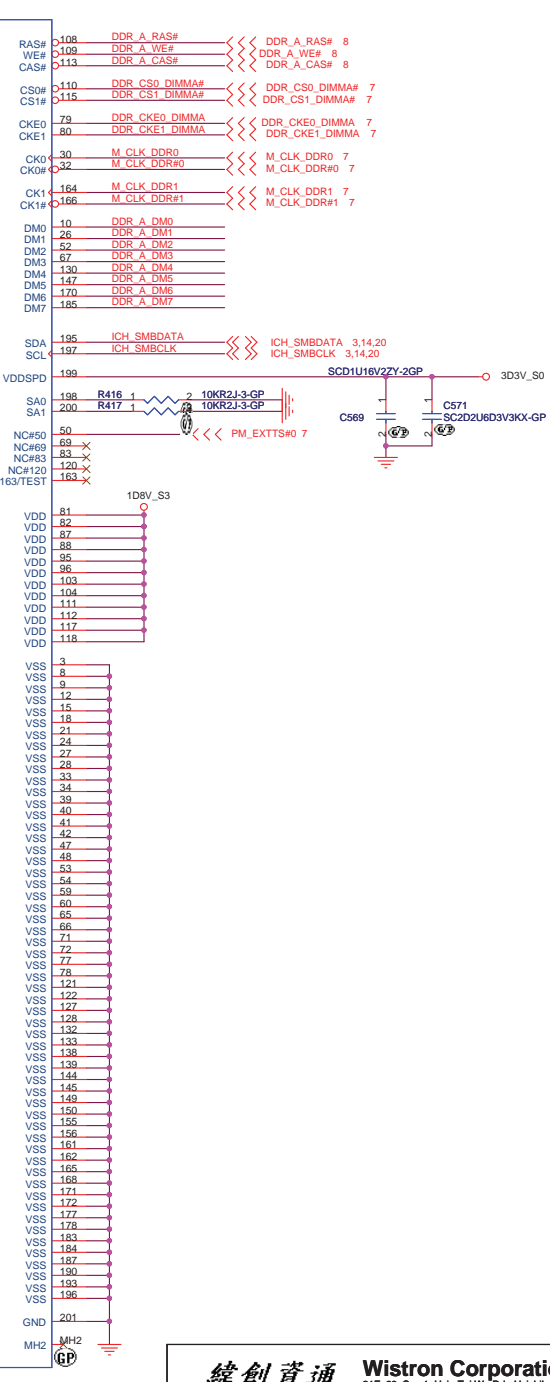
<http://hobi-elektronika.net>

DM2	
DDR A MA0	102
DDR A MA1	101
DDR A MA2	100
DDR A MA3	99
DDR A MA4	98
DDR A MA5	97
DDR A MA6	96
DDR A MA7	95
DDR A MA8	94
DDR A MA9	93
DDR A MA10	92
DDR A MA11	91
DDR A MA12	90
DDR A MA13	89
DDR A MA14	88
DDR A BS2	85
DDR A BS0	107
DDR A BS1	106
DDR A D0	5
DDR A D1	17
DDR A D2	19
DDR A D3	17
DDR A D4	4
DDR A D5	14
DDR A D6	16
DDR A D7	23
DDR A D8	29
DDR A D9	35
DDR A D10	37
DDR A D11	22
DDR A D12	20
DDR A D13	20
DDR A D14	36
DDR A D15	38
DDR A D16	43
DDR A D17	45
DDR A D18	55
DDR A D19	57
DDR A D20	44
DDR A D21	46
DDR A D22	56
DDR A D23	58
DDR A D24	61
DDR A D25	63
DDR A D26	75
DDR A D27	73
DDR A D28	75
DDR A D29	64
DDR A D30	74
DDR A D31	76
DDR A D32	123
DDR A D33	125
DDR A D34	135
DDR A D35	137
DDR A D36	124
DDR A D37	126
DDR A D38	134
DDR A D39	136
DDR A D40	141
DDR A D41	143
DDR A D42	151
DDR A D43	153
DDR A D44	140
DDR A D45	142
DDR A D46	152
DDR A D47	154
DDR A D48	157
DDR A D49	159
DDR A D50	173
DDR A D51	175
DDR A D52	158
DDR A D53	160
DDR A D54	174
DDR A D55	176
DDR A D56	179
DDR A D57	181
DDR A D58	189
DDR A D59	191
DDR A D60	180
DDR A D61	182
DDR A D62	192
DDR A D63	194

DDR A DQS#0	110
DDR A DQS#1	29
DDR A DQS#2	49
DDR A DQS#3	68
DDR A DQS#4	129
DDR A DQS#5	146
DDR A DQS#6	167
DDR A DQS#7	186
DDR A DQS0	13
DDR A DQS1	31
DDR A DQS2	51
DDR A DQS3	70
DDR A DQS4	131
DDR A DQS5	148
DDR A DQS6	169
DDR A DQS7	188

DDR A DQS0	13
DDR A DQS1	31
DDR A DQS2	51
DDR A DQS3	70
DDR A DQS4	131
DDR A DQS5	148
DDR A DQS6	169
DDR A DQS7	188
DDR A DQS0	13
DDR A DQS1	31
DDR A DQS2	51
DDR A DQS3	70
DDR A DQS4	131
DDR A DQS5	148
DDR A DQS6	169
DDR A DQS7	188

DDR2-200P-20-GP-U



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Title

DDR2-SODIMM SLOT1

Size

Document Number

Customer

Pamirs-Discrete

Date

Wednesday, September 12, 2007

Sheet

13

of

47

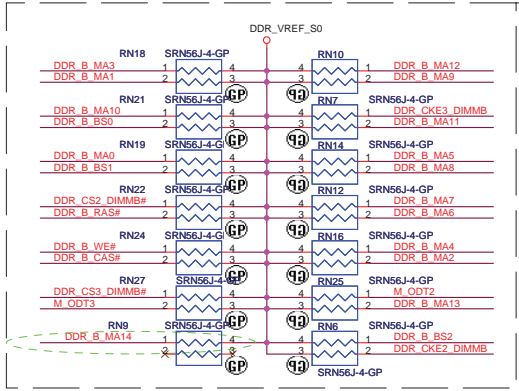
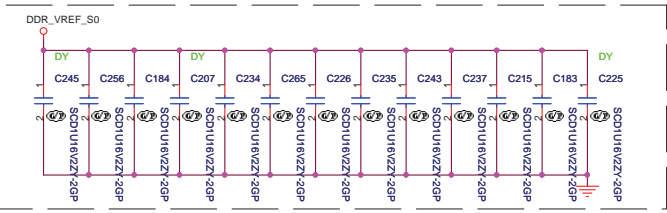
Rev

SA

Layout Note:
Place near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



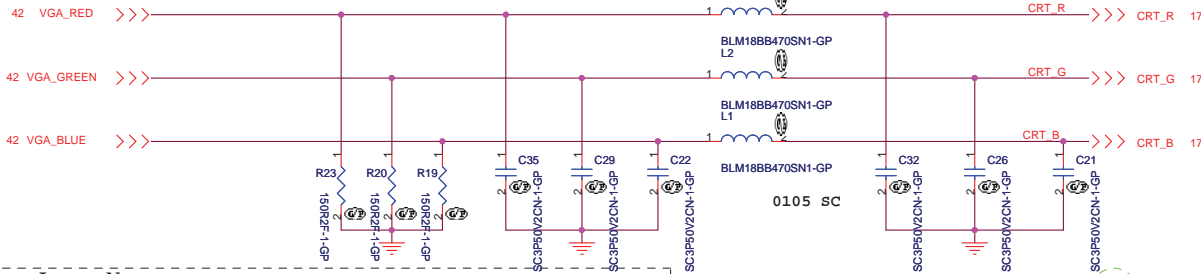
Layout Note:
Place these resistors
closely DM2,all
trace length Max=1.5"

<http://hobi-elektronika.net>

	DDR_B_MA0	102	A0
	DDR_B_MA1	101	A1
	DDR_B_MA2	100	A2
	DDR_B_MA3	99	A3
	DDR_B_MA4	98	A4
	DDR_B_MA5	97	A5
	DDR_B_MA6	94	A6
	DDR_B_MA7	92	A7
	DDR_B_MA8	93	A8
	DDR_B_MA9	91	A9
	DDR_B_MA10	105	A10/AP
	DDR_B_MA11	90	A11
	DDR_B_MA12	89	A12
	DDR_B_MA13	116	A13
7 DDR_B_MA14	DDR_B_MA14	86	A14
<< >>			A15
	DDR_B_BS2	84	A16/BA2
		85	
	DDR_B_BS0	107	BA0
	DDR_B_BS1	106	BA1
	DDR_B_D0	5	DO0
	DDR_B_D1	7	DO1
	DDR_B_D2	17	DO2
	DDR_B_D3	19	DO3
	DDR_B_D4	4	DO4
	DDR_B_D5	6	DO5
	DDR_B_D6	14	DO6
	DDR_B_D7	10	DO7
	DDR_B_D8	23	DO8
	DDR_B_D9	25	DO9
	DDR_B_D10	37	DO10
	DDR_B_D11	31	DO11
	DDR_B_D12	20	DO12
	DDR_B_D13	22	DO13
	DDR_B_D14	36	DO14
	DDR_B_D15	38	DO15
	DDR_B_D16	43	DO16
	DDR_B_D17	45	DO17
	DDR_B_D18	55	DO18
	DDR_B_D19	57	DO19
	DDR_B_D20	44	DO20
	DDR_B_D21	46	DO21
	DDR_B_D22	56	DO22
	DDR_B_D23	58	DO23
	DDR_B_D24	61	DO24
	DDR_B_D25	63	DO25
	DDR_B_D26	73	DO26
	DDR_B_D27	75	DO27
	DDR_B_D28	62	DO28
	DDR_B_D29	64	DO29
	DDR_B_D30	74	DO30
	DDR_B_D31	76	DO31
	DDR_B_D32	123	DO32
	DDR_B_D33	125	DO33
	DDR_B_D34	135	DO34
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	DDR_B_D38	134	DO38
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	DDR_B_D40	141	DO40
	DDR_B_D41	143	DO41
	DDR_B_D42	151	DO42
	DDR_B_D43	153	DO43
	DDR_B_D44	149	DO44
	DDR_B_D45	147	DO45
	DDR_B_D46	152	DO46
	DDR_B_D47	154	DO47
	DDR_B_D48	157	DO48
	DDR_B_D49	159	DO49
	DDR_B_D50	173	DO50
	DDR_B_D51	175	DO51
	DDR_B_D52	158	DO52
	DDR_B_D53	160	DO53
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	DDR_B_D56	179	DO56
	DDR_B_D57	181	DO57
	DDR_B_D58	189	DO58
	DDR_B_D59	191	DO59
	DDR_B_D60	180	DO60
	DDR_B_D61	182	DO61
	DDR_B_D62	192	DO62
	DDR_B_D63	194	DO63
	DDR_B_DQS#0	11	DO64
	DDR_B_DQS#1	25	DO65
	DDR_B_DQS#2	49	DO66
	DDR_B_DQS#3	69	DO67
	DDR_B_DQS#4	128	DO68
	DDR_B_DQS#5	146	DO69
	DDR_B_DQS#6	167	DO70
	DDR_B_DQS#7	196	DO71
	DDR_B_DQS#0	13	DO80
	DDR_B_DQS#1	31	DO81
	DDR_B_DQS#2	51	DO82
	DDR_B_DQS#3	70	DO83
	DDR_B_DQS#4	131	DO84
	DDR_B_DQS#5	148	DO85
	DDR_B_DQS#6	169	DO86
	DDR_B_DQS#7	188	DO87
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	DDR_B_DQS#2	114	DO92
	DDR_B_DQS#3	119	DO93
	DDR_B_DQS#4	114	DO94
	DDR_B_DQS#5	119	DO95
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	DDR_B_DQS#7	119	DO97
	DDR_B_DQS#0	114	DO100
	DDR_B_DQS#1	119	DO101
	DDR_B_DQS#2	114	DO102
	DDR_B_DQS#3	119	DO103
	DDR_B_DQS#4	114	DO104
	DDR_B_DQS#5	119	DO105
	DDR_B_DQS#6	114	DO106
	DDR_B_DQS#7	119	DO107
	DDR_B_DQS#0	114	DO110
	DDR_B_DQS#1	119	DO111
	DDR_B_DQS#2	114	DO112
	DDR_B_DQS#3	119	DO113
	DDR_B_DQS#4	114	DO114
	DDR_B_DQS#5	119	DO115
	DDR_B_DQS#6	114	DO116
	DDR_B_DQS#7	119	DO117
	DDR_B_DQS#0	114	DO120
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	DDR_B_DQS#6	114	DO126
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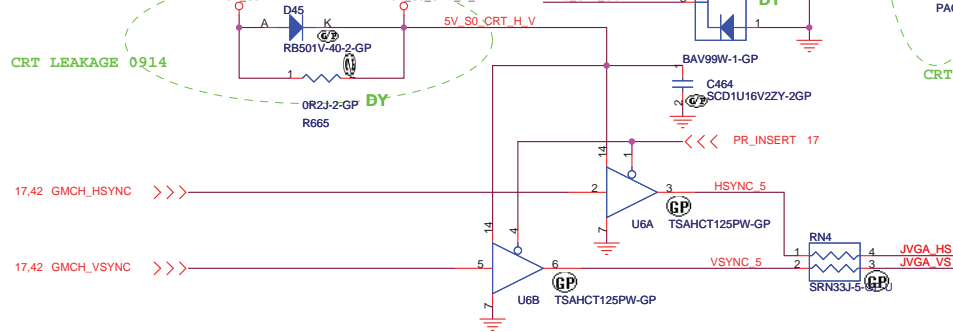
CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector



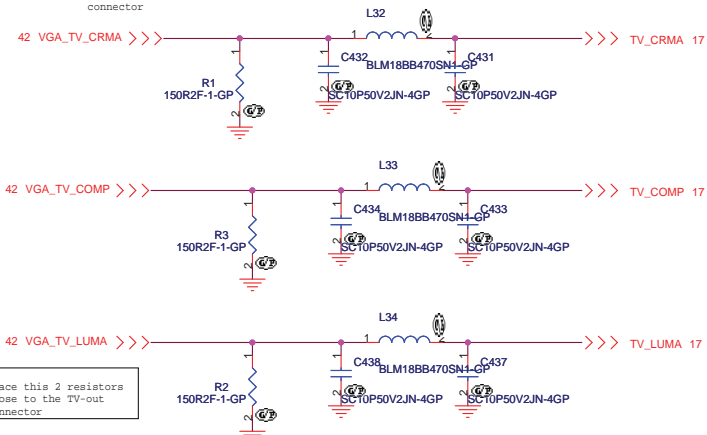
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

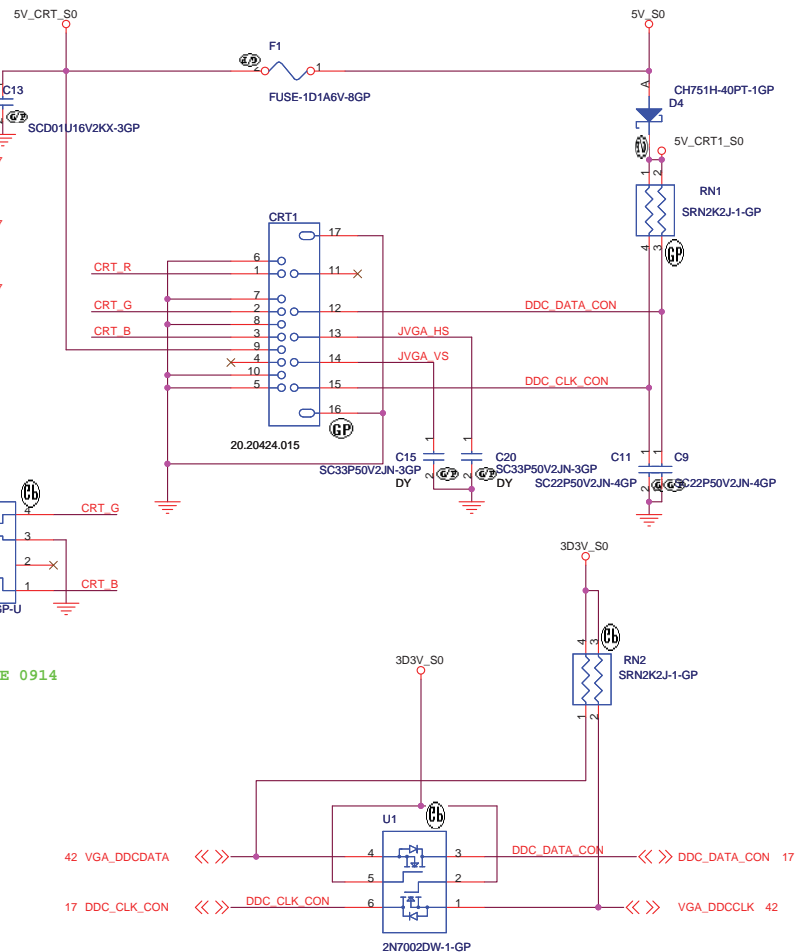
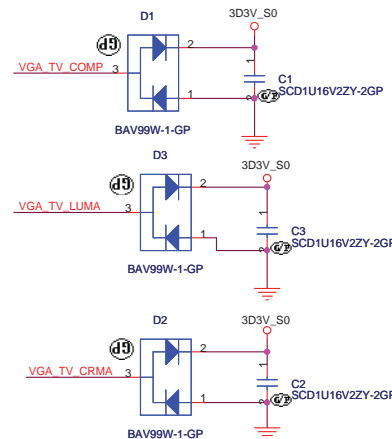
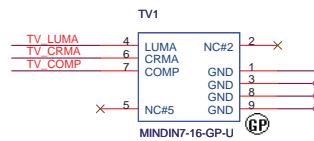


TV OUT CONN

connector



Place this 2 resistors
close to the TV-out
connector

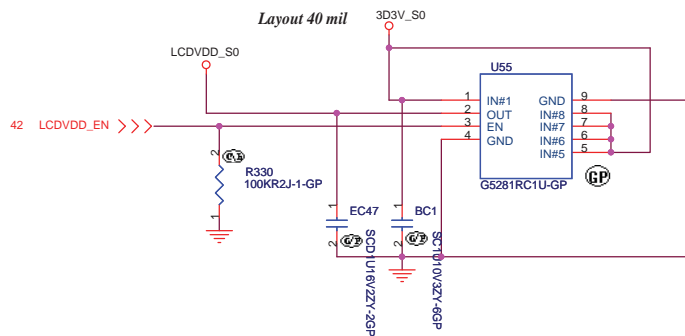
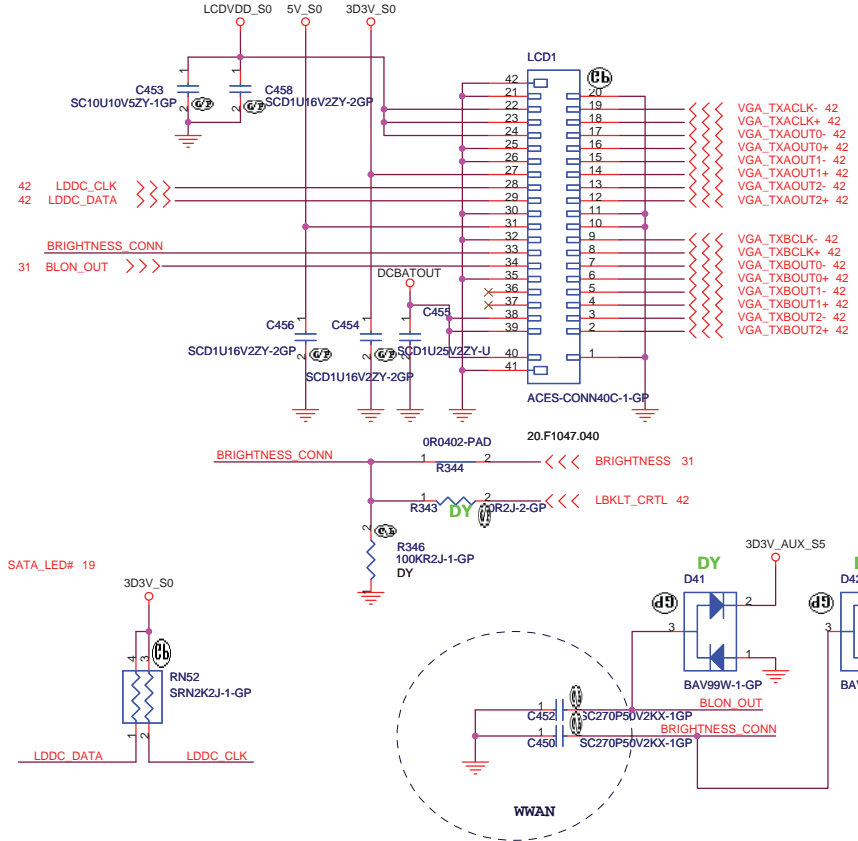
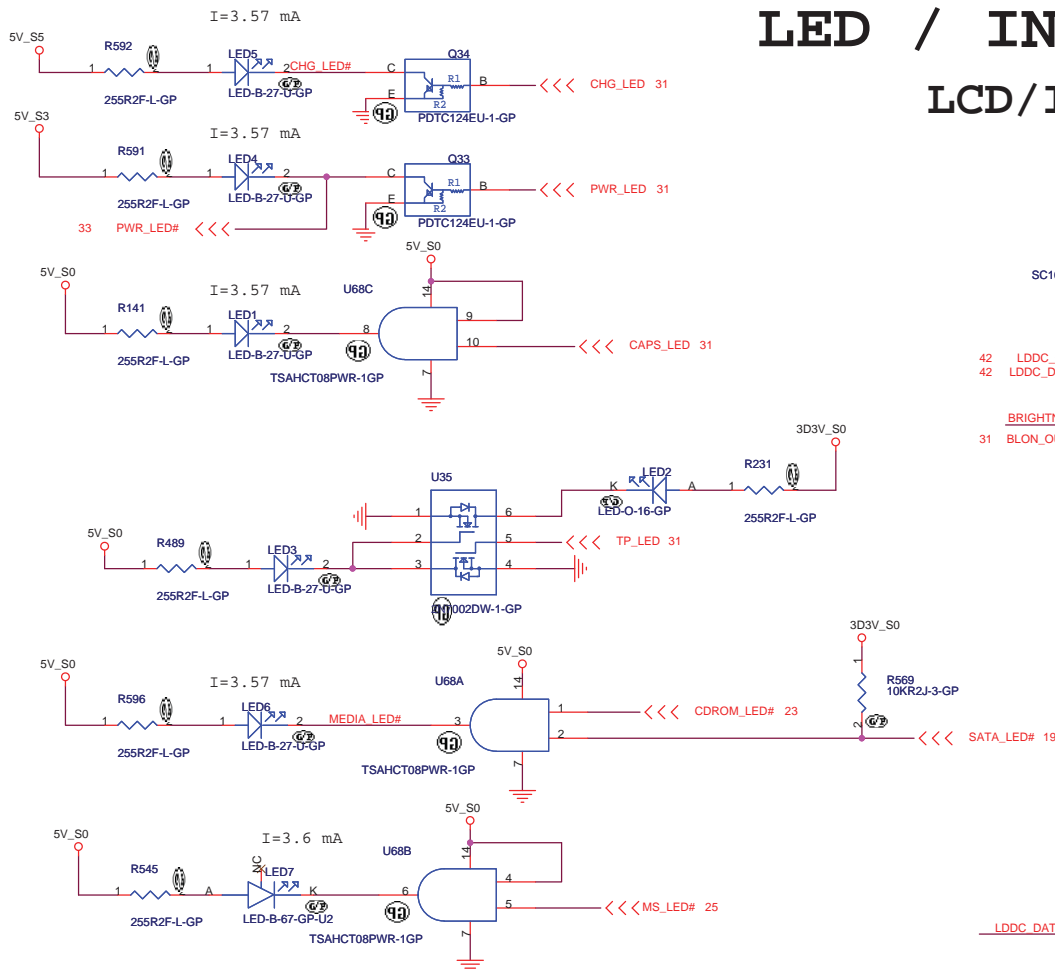


5V @ ext. CRT side

<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>			
Title			
<div>CRT/TV Connector</div>			
Size	Document Number	Rev	
A3		SA	
Date:	Friday, September 14, 2007	Sheet	15 of 47

LED / INVERTER INTERFACE

LCD/INV CONN

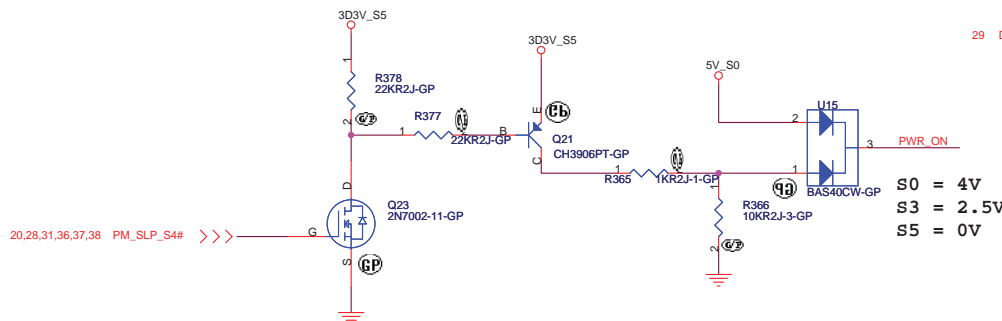
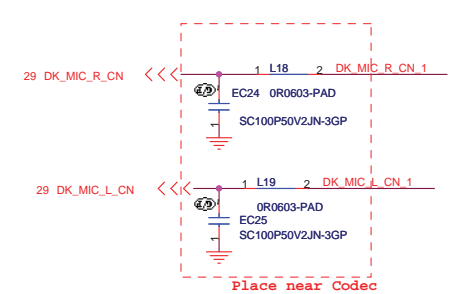
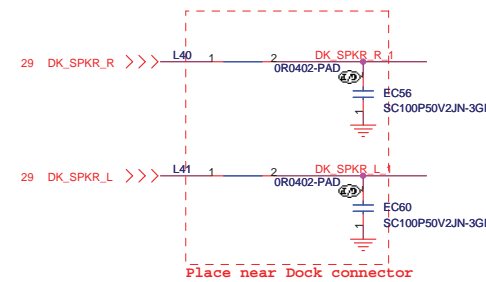
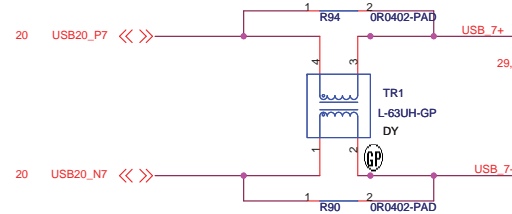
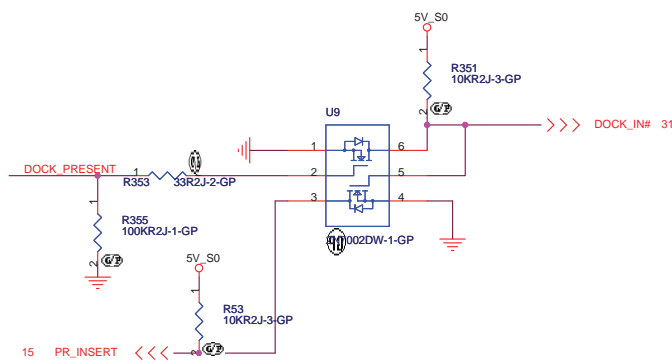
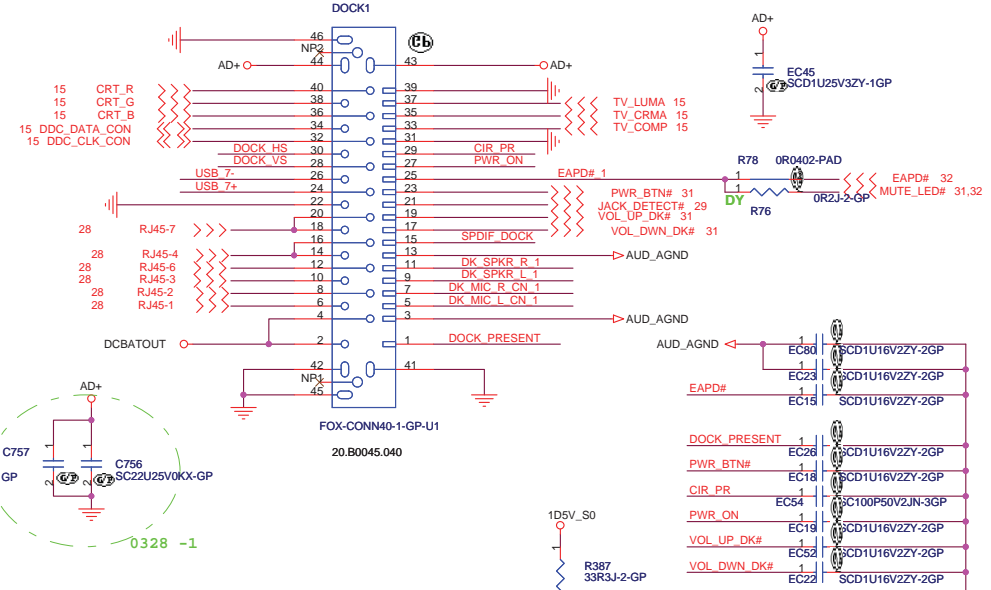
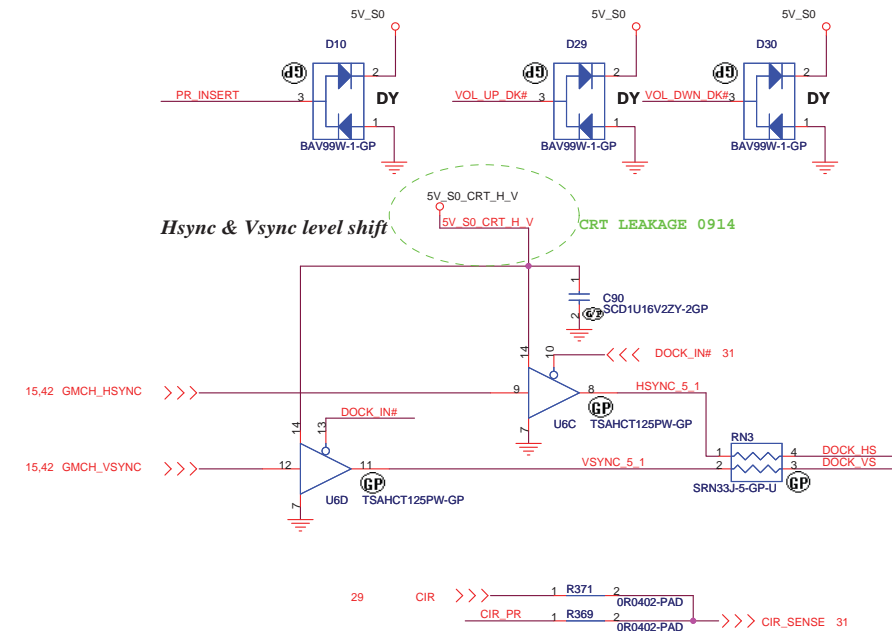


<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

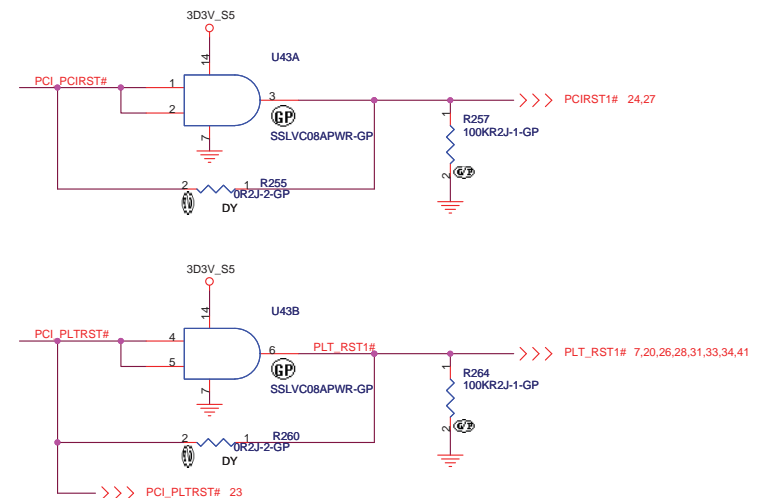
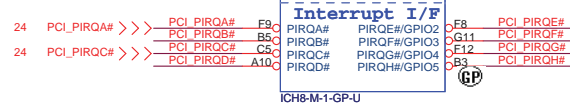
LCD/Inverter Connector		
Size	Document Number	Rev
Custom	Pamirs-Discrete	SA
Date: Wednesday, September 12, 2007	Sheet 16 of 47	

Docking Connector

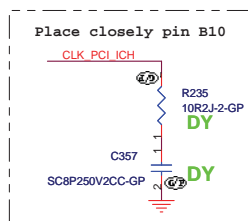


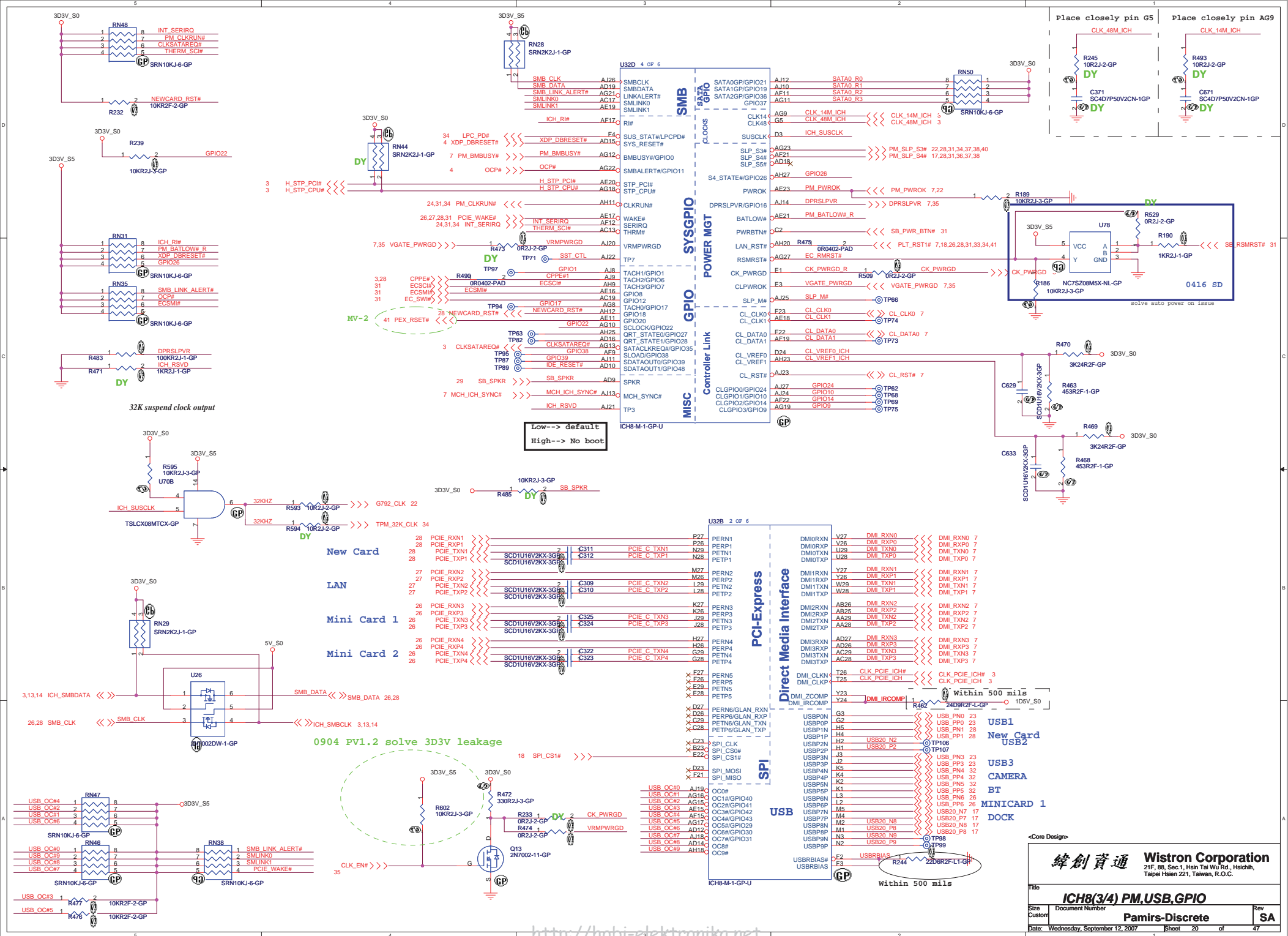
S0 = 4V
S3 = 2.5V
S5 = 0V

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	Board to board conn/ Docking		
Size A3	Document Number	Pamirs-Discrete	Rev SA
Date: Friday, September 14, 2007	Sheet 17	of 47	

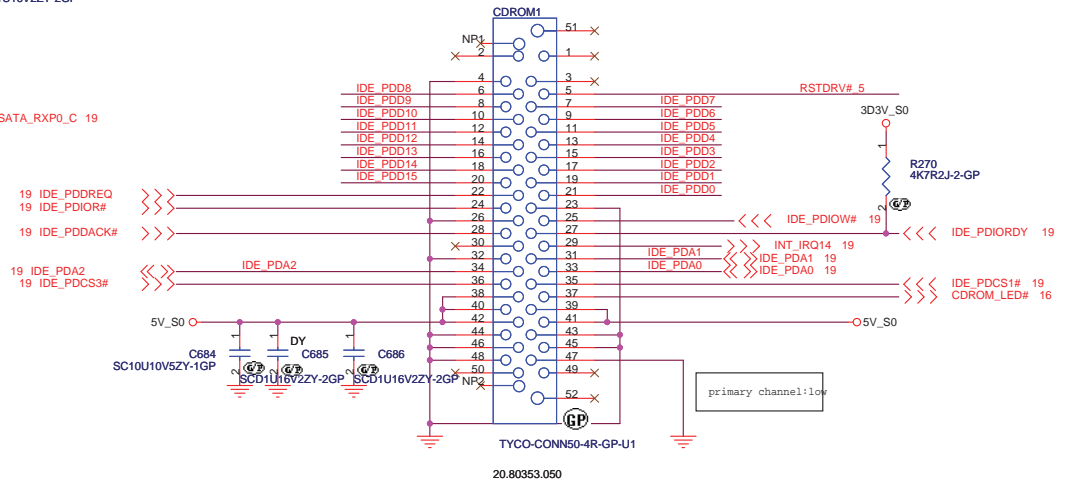


Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

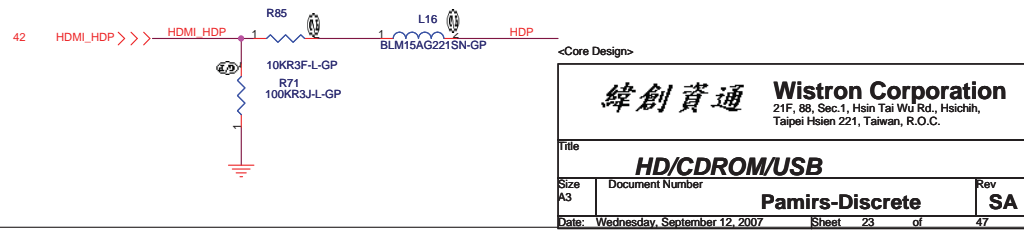
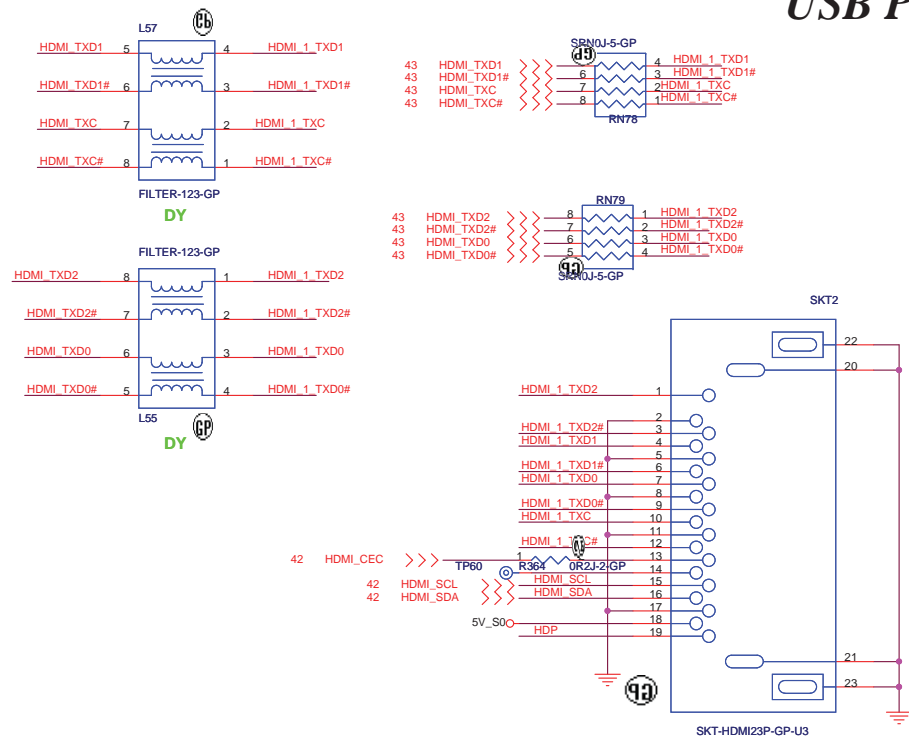


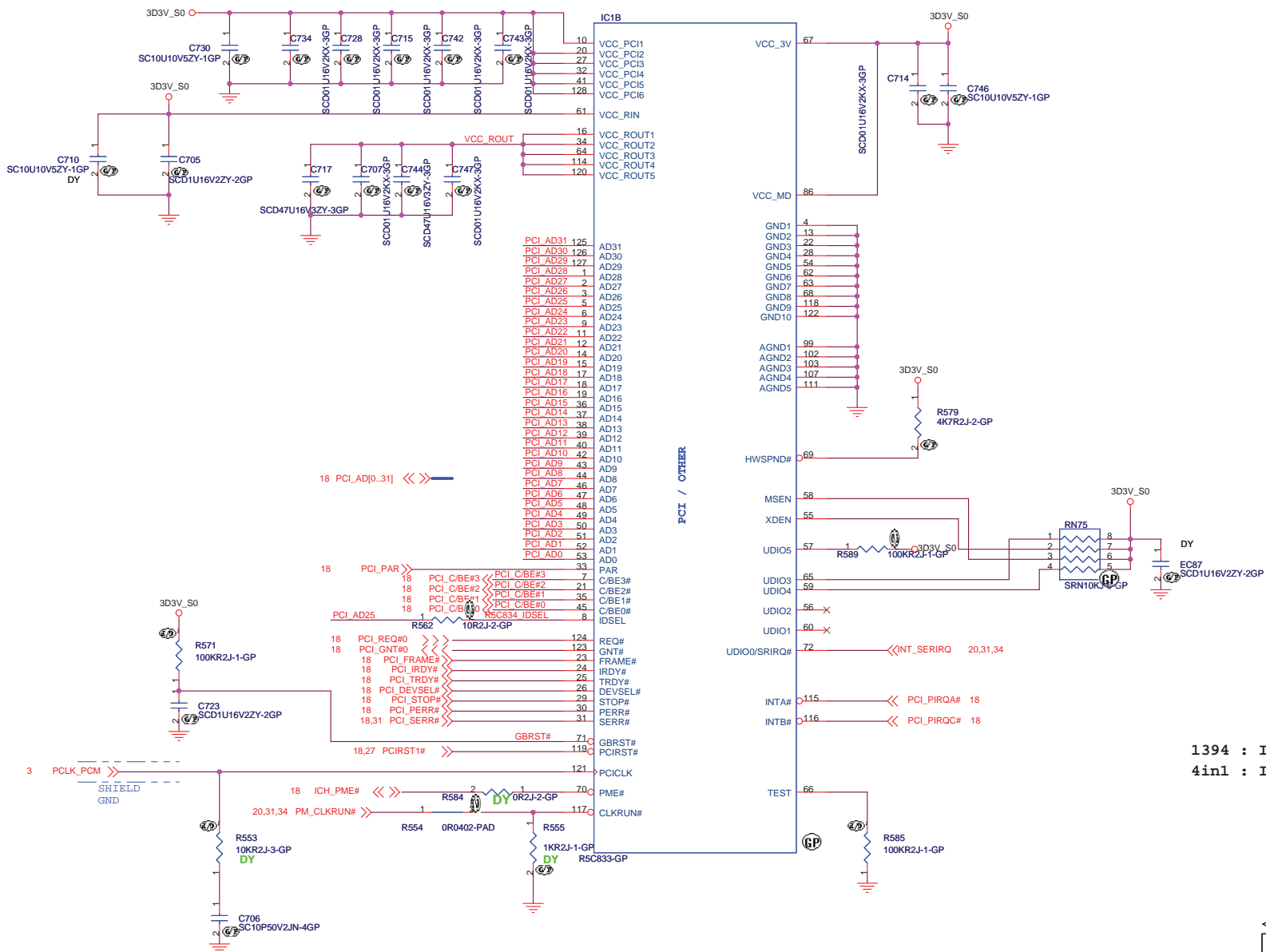


CD-ROM CONNECTOR



20. F0735.010





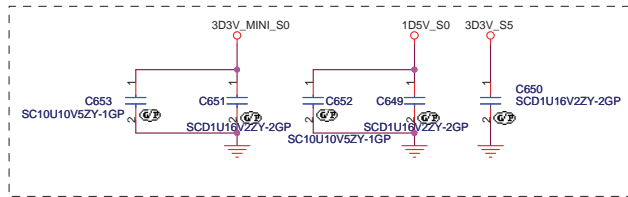
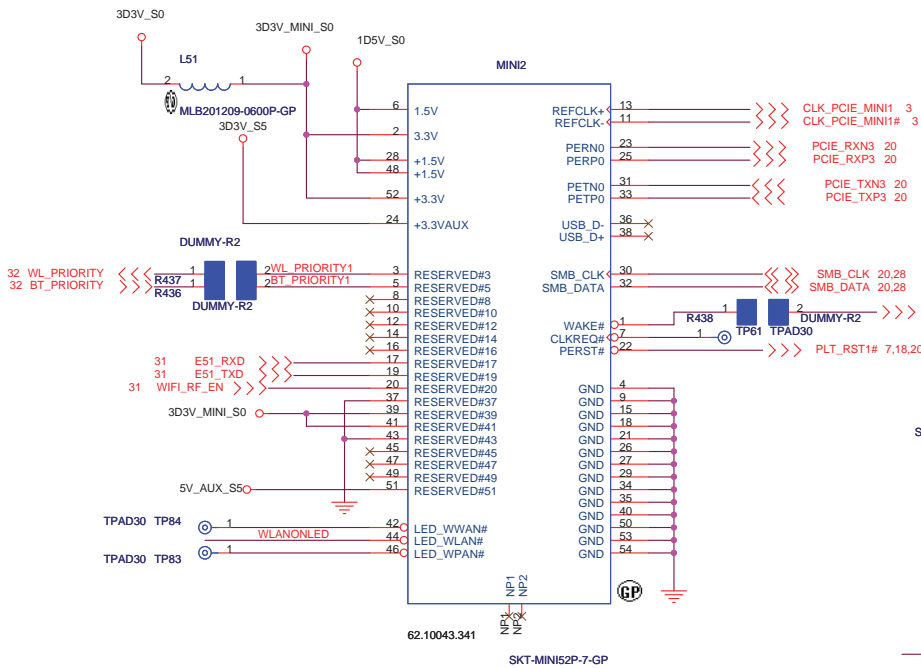
1394 : INTA#
4in1 : INTB#

<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
R5C832/PCI		
Size	Document Number	Rev
A3		SA
Date: Thursday, September 13, 2007	Sheet 24 of 47	

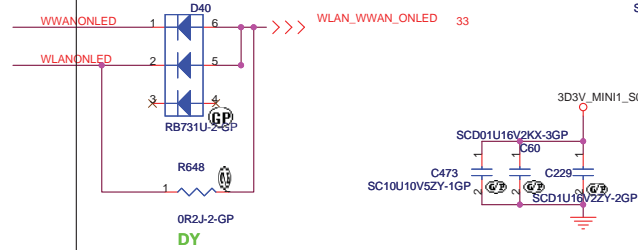
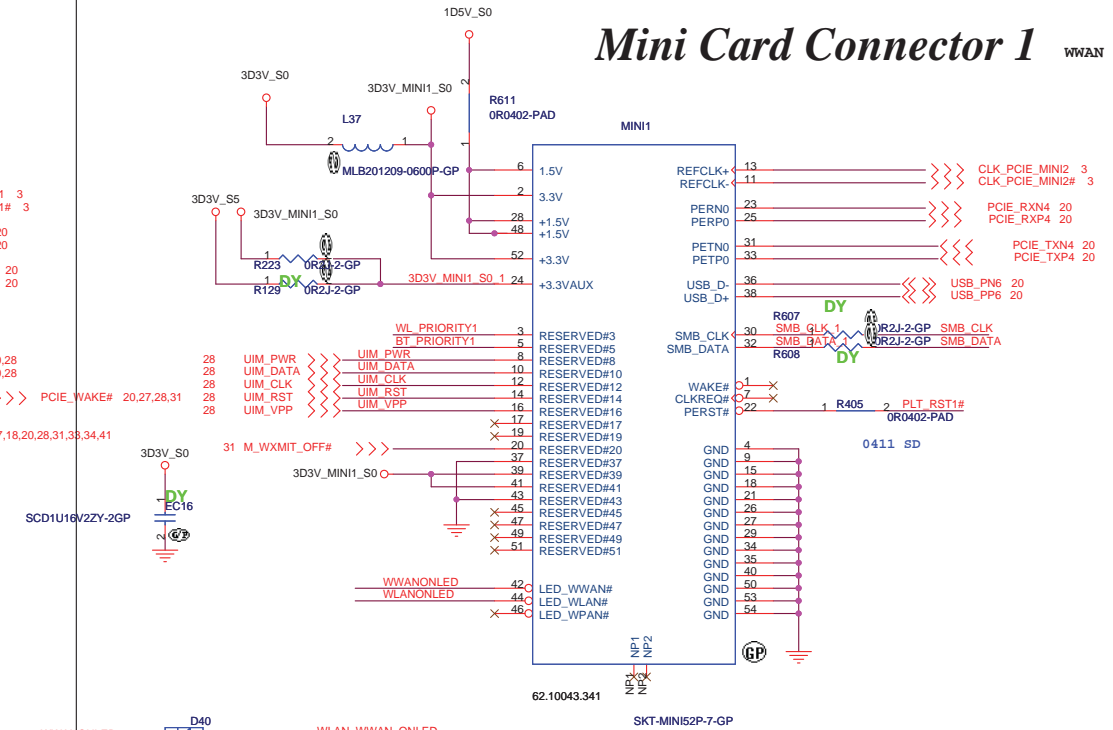
Mini Card Connector 2

Wireless card



Mini Card Connector 1

WWAN

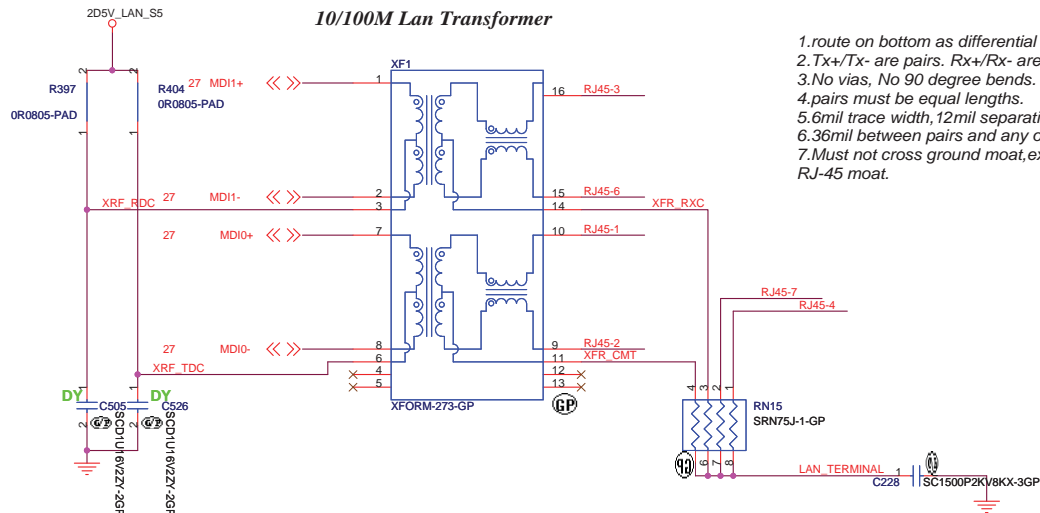


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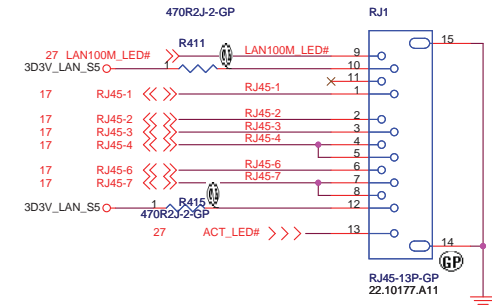
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MINI CARD CONN.		
Size	Document Number	Pamirs-Discrete	Rev
A3			SA

Date: Wednesday, September 12, 2007 Sheet 26 of 47

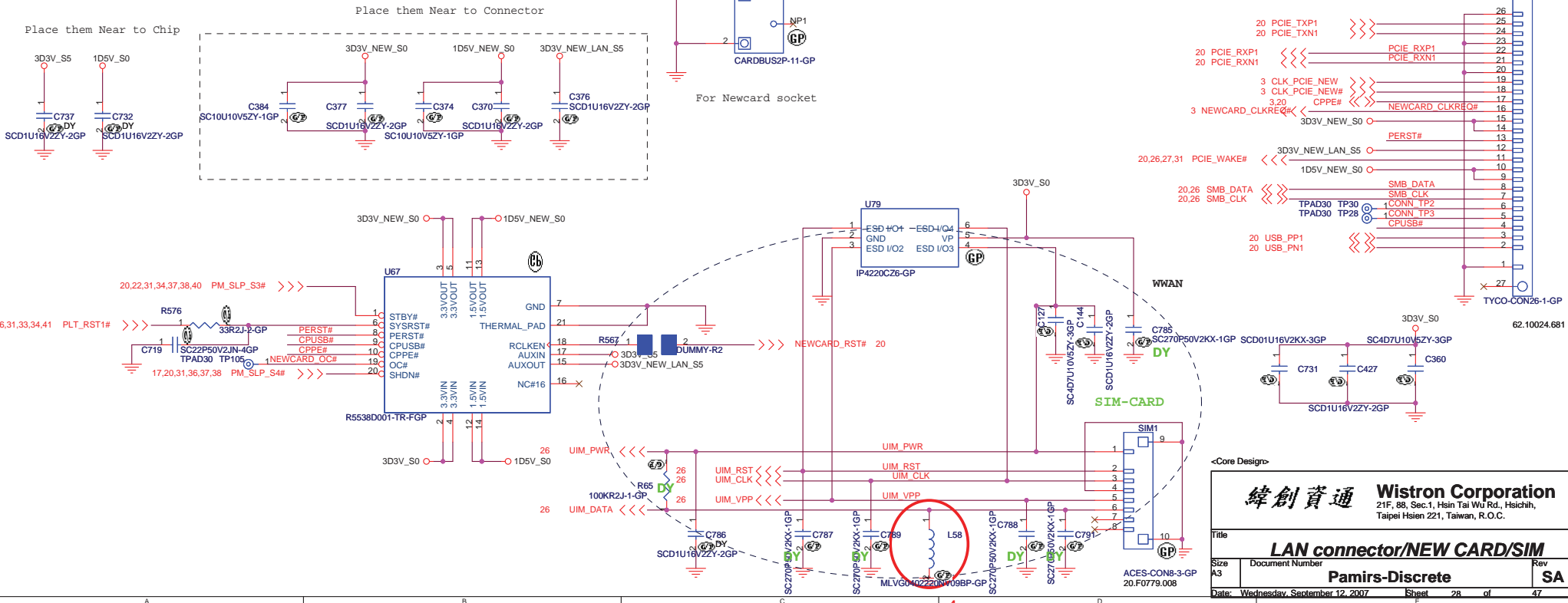


PIN09 : GREEN
 PIN11 : ORANGE
 PIN13 : YELLOW



Green : Link up
 Blinking : TX/RX activity

NEWCARD Connector



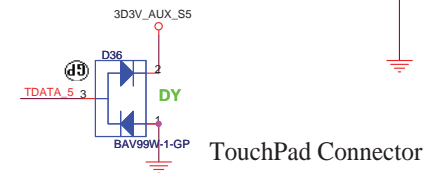
CAMERA

Internal Keyboard Connector

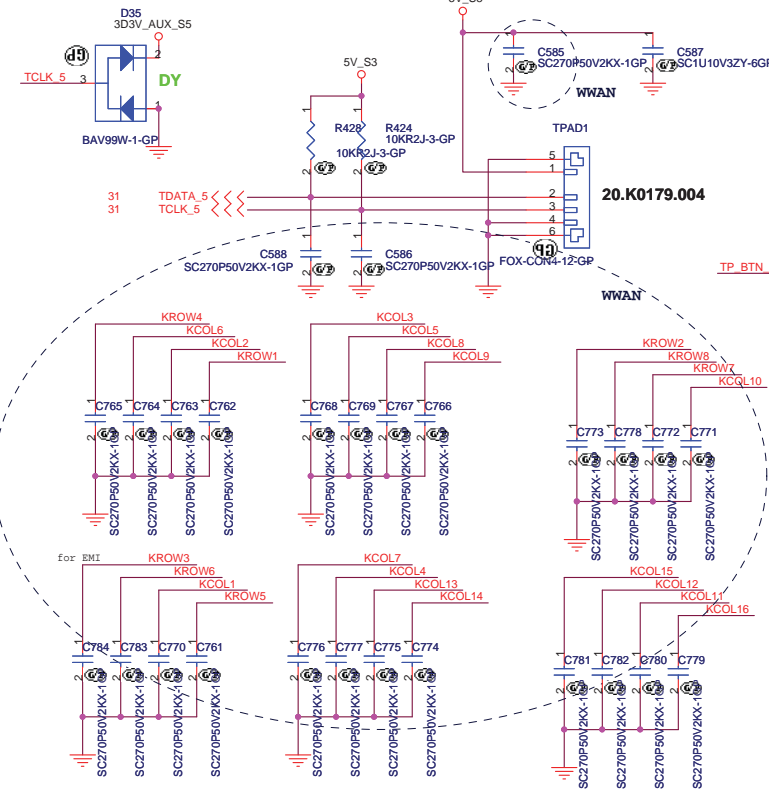
31 KROW[1..8] <<< 
31 KCOL[1..16] <<< 

Keyboard matrix (from vendor)

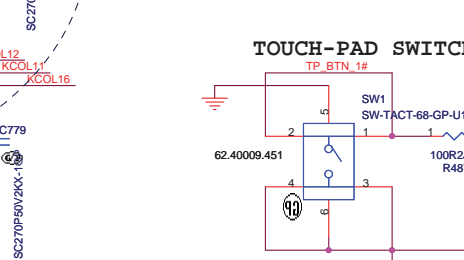
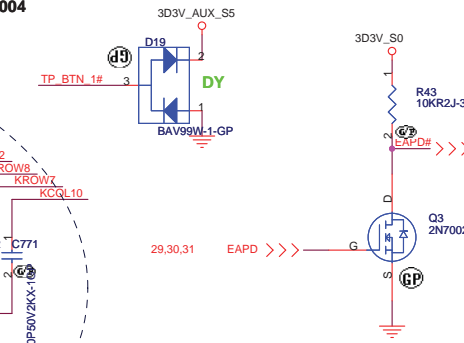
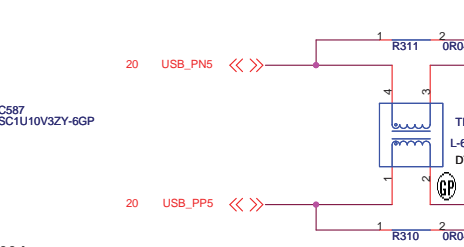
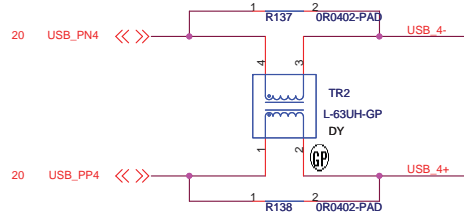
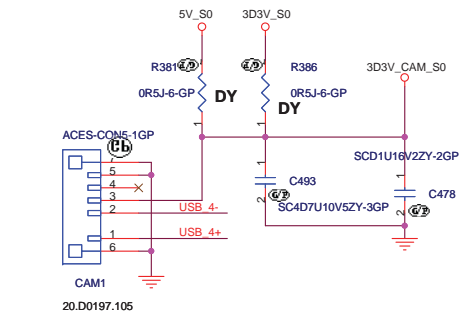
	US	Eur	Jap
MATRIXID1#	0	1	0
MATRIXID2#	0	0	1



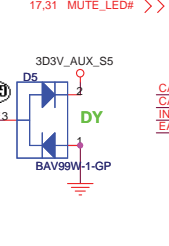
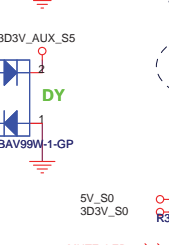
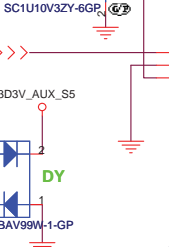
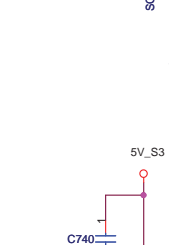
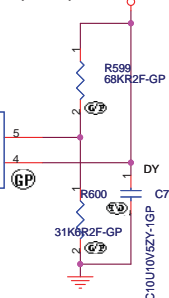
TouchPad Connector



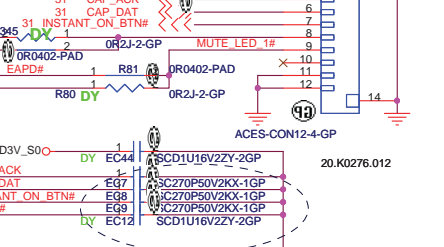
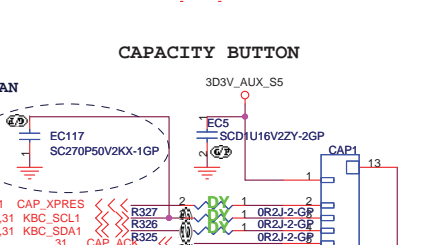
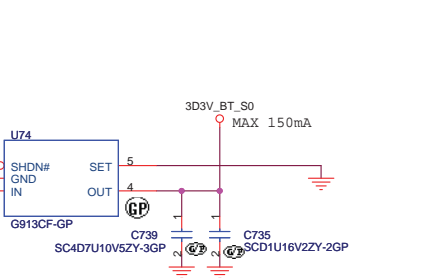
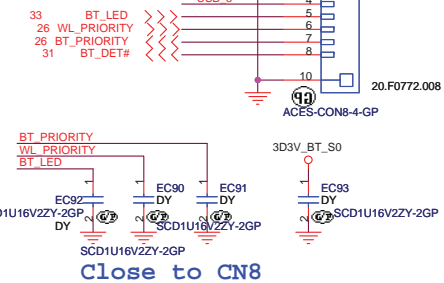
CAMERA



(3.3V)



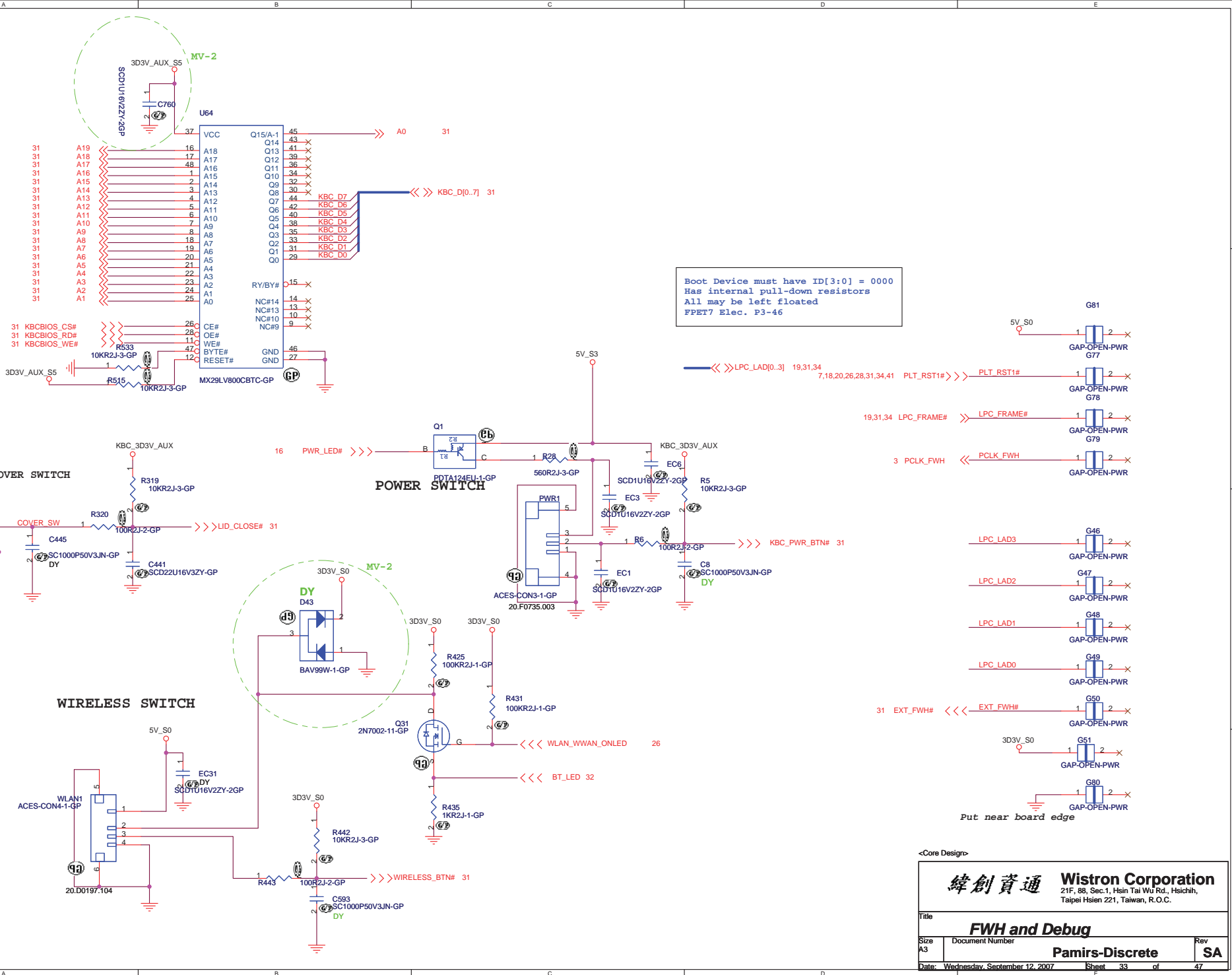
Blue thumb



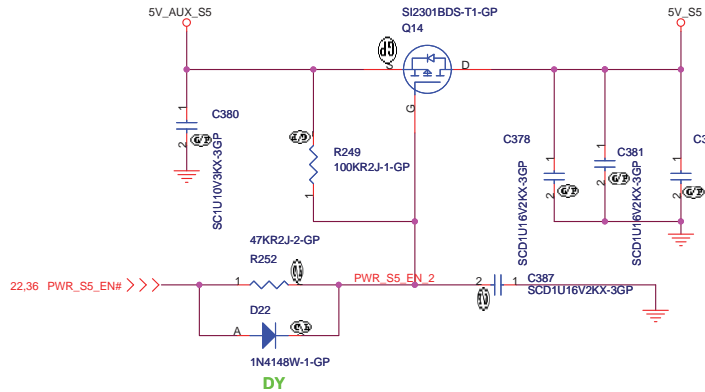
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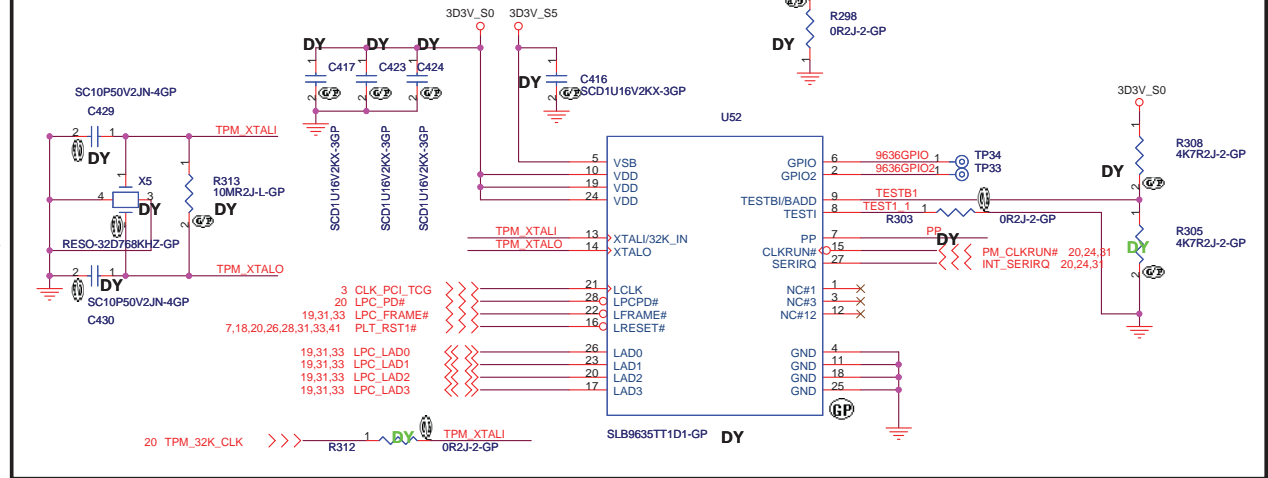
KeyBoard-CONN		
Size A3	Document Number	Rev SA
Date: Wednesday, September 12, 2007	Sheet 32 of 47	



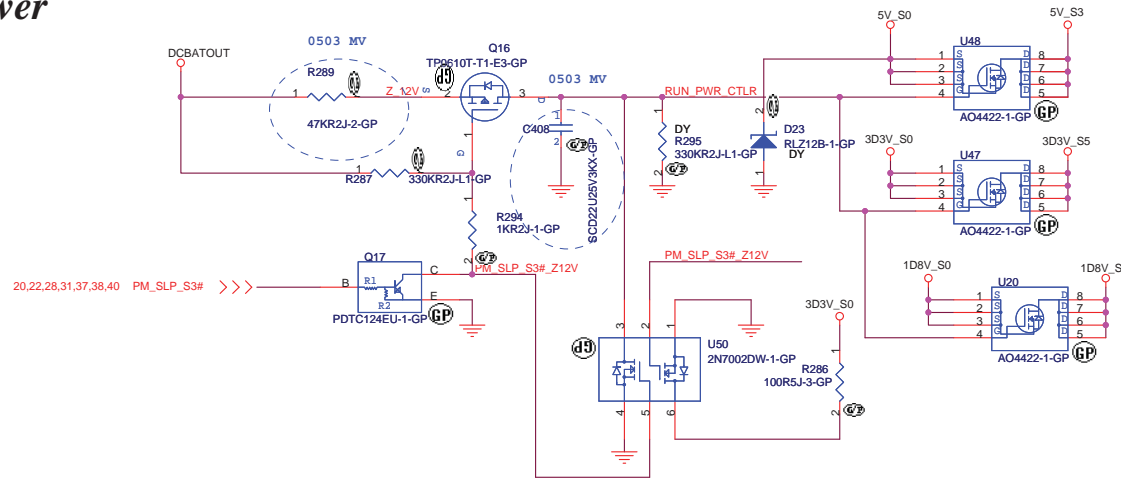
5V_AUX_S5 TO 5V_S5



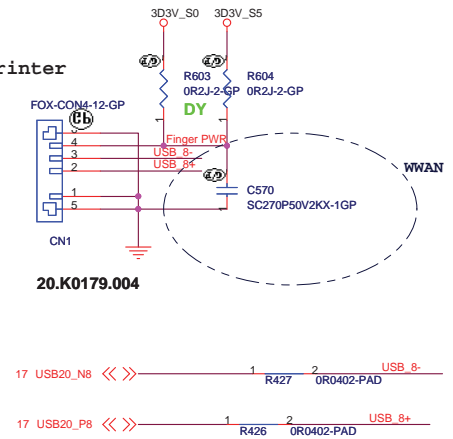
TPM 1.2



Run Power

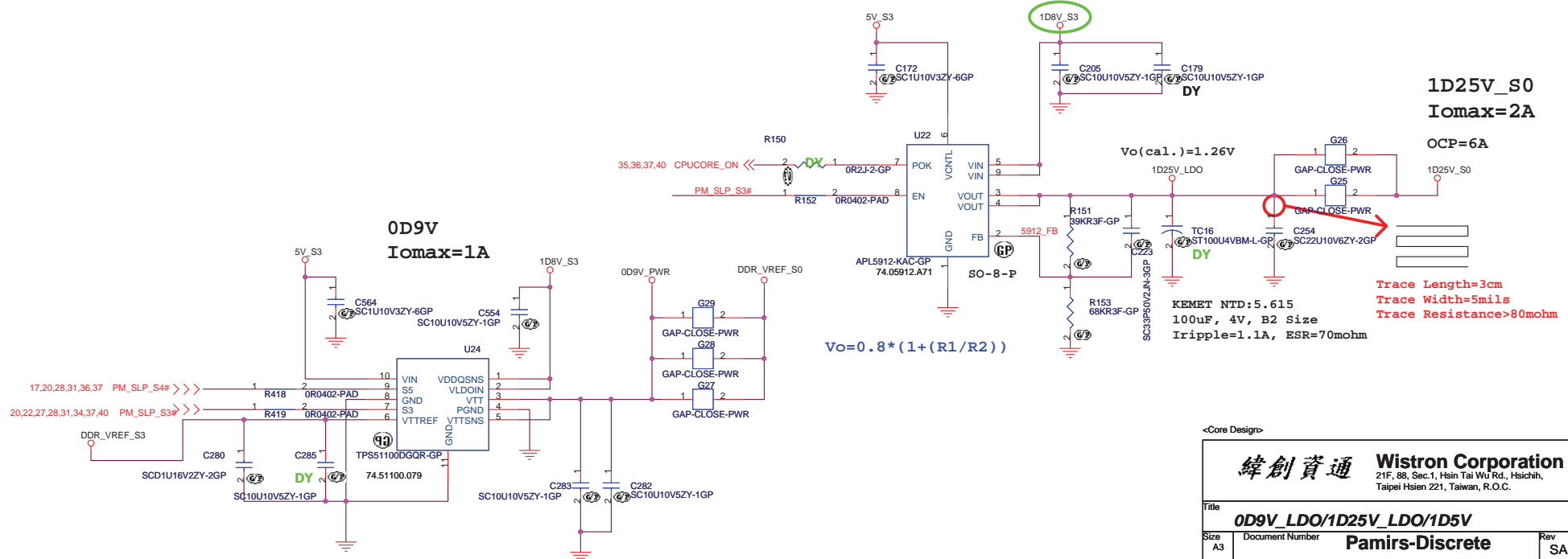
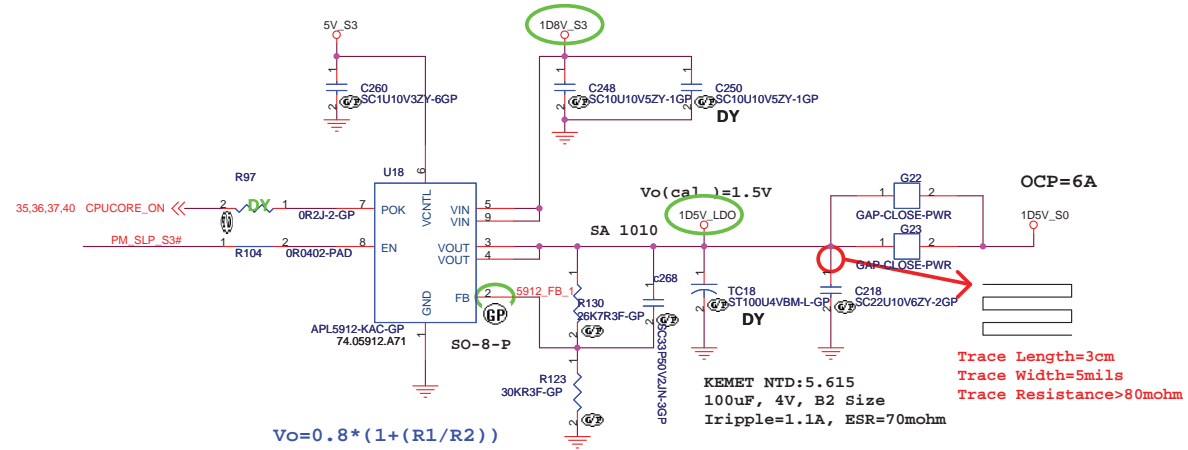


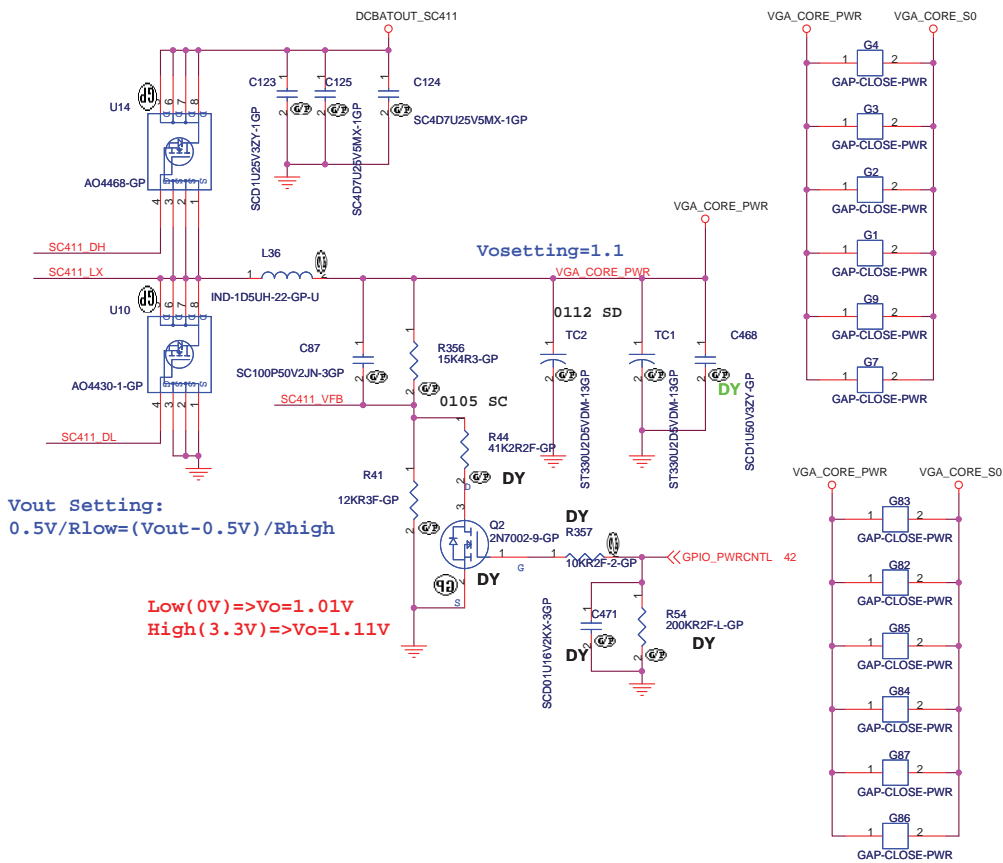
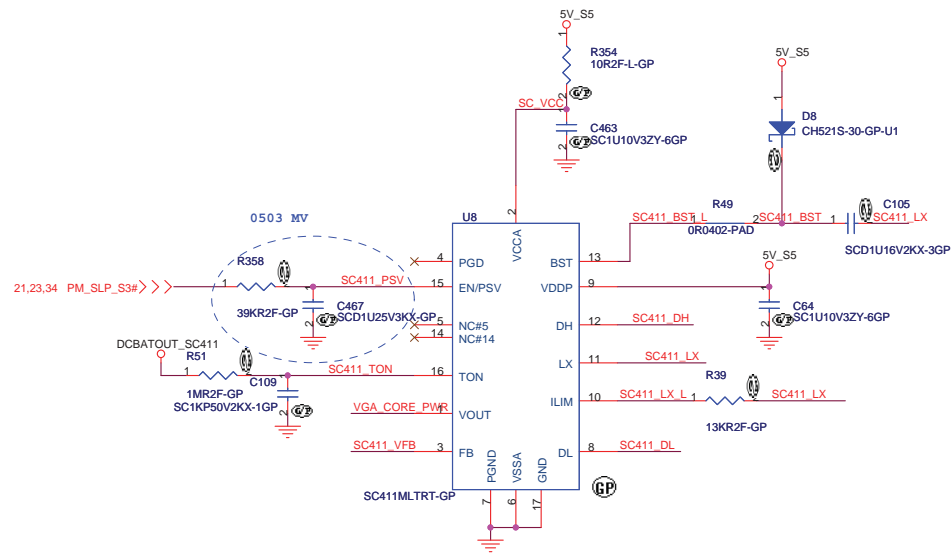
Finger Printer



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Title			
PWRPLANE&RESETLOGIC			
Size A3	Document Number	Pamirs-Discrete	Rev SA
Date:	Wednesday, September 12, 2007	Sheet 34	of 47

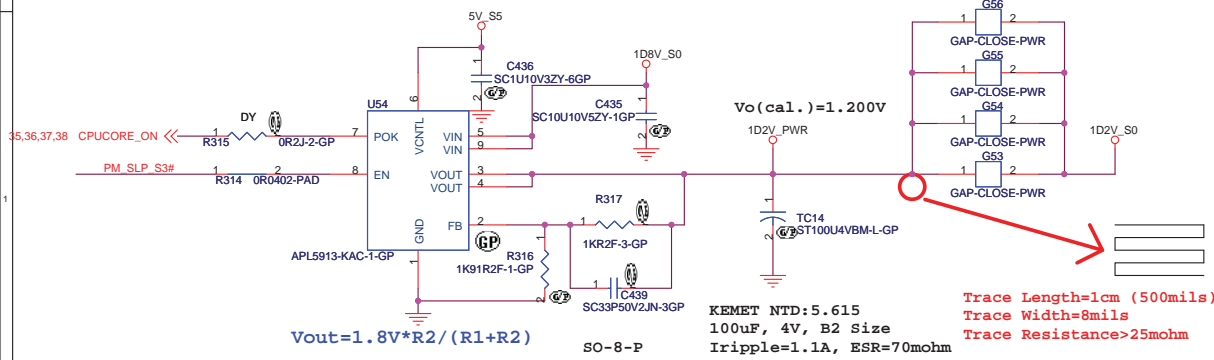




Vout Setting:
 $0.5V/R_{low} = (V_{out} - 0.5V) / R_{high}$

Low(0V) => Vo=1.01V
 High(3.3V) => Vo=1.11V

1D2V_S0
 Iomax=3A

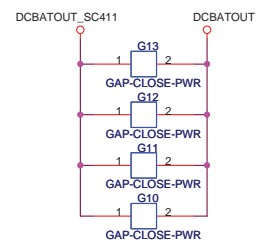
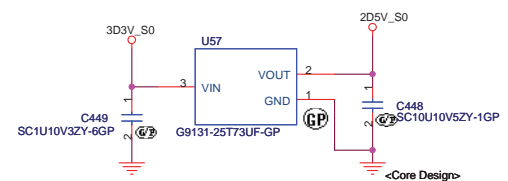


$V_{out} = 1.8V \cdot R2 / (R1 + R2)$

KEMET NTD:5.615
 100uF, 4V, B2 Size
 Iripple=1.1A, ESR=70mohm

Trace Length=1cm (500mils)
 Trace Width=8mils
 Trace Resistance>25mohm

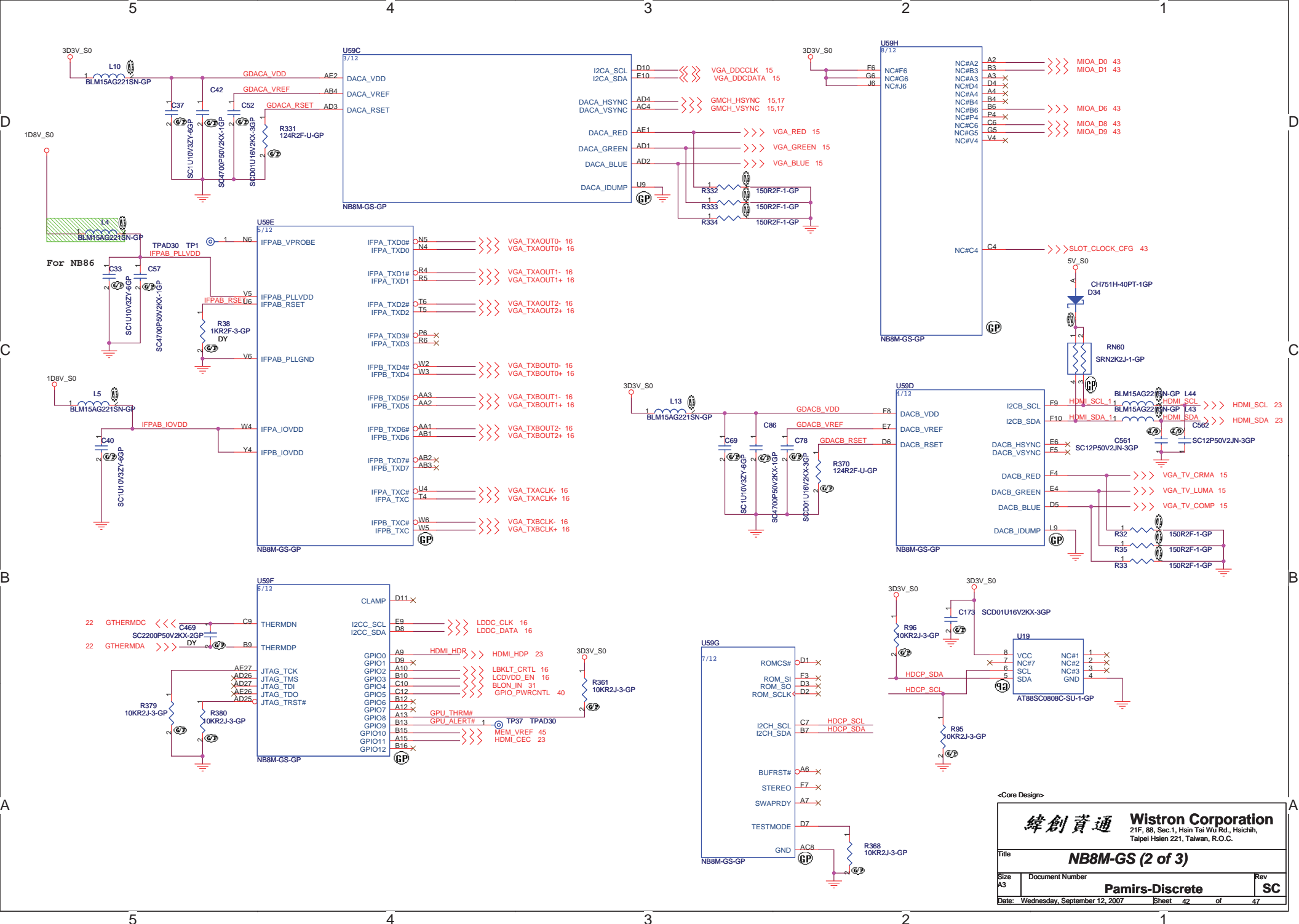
2D5V_S0
 Iomax=300mA



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Title VGA CORE 1V		
Size A3	Document Number Pamirs-Discrete	Rev SA
Date: Wednesday, September 12, 2007 Sheet 40 of 47		





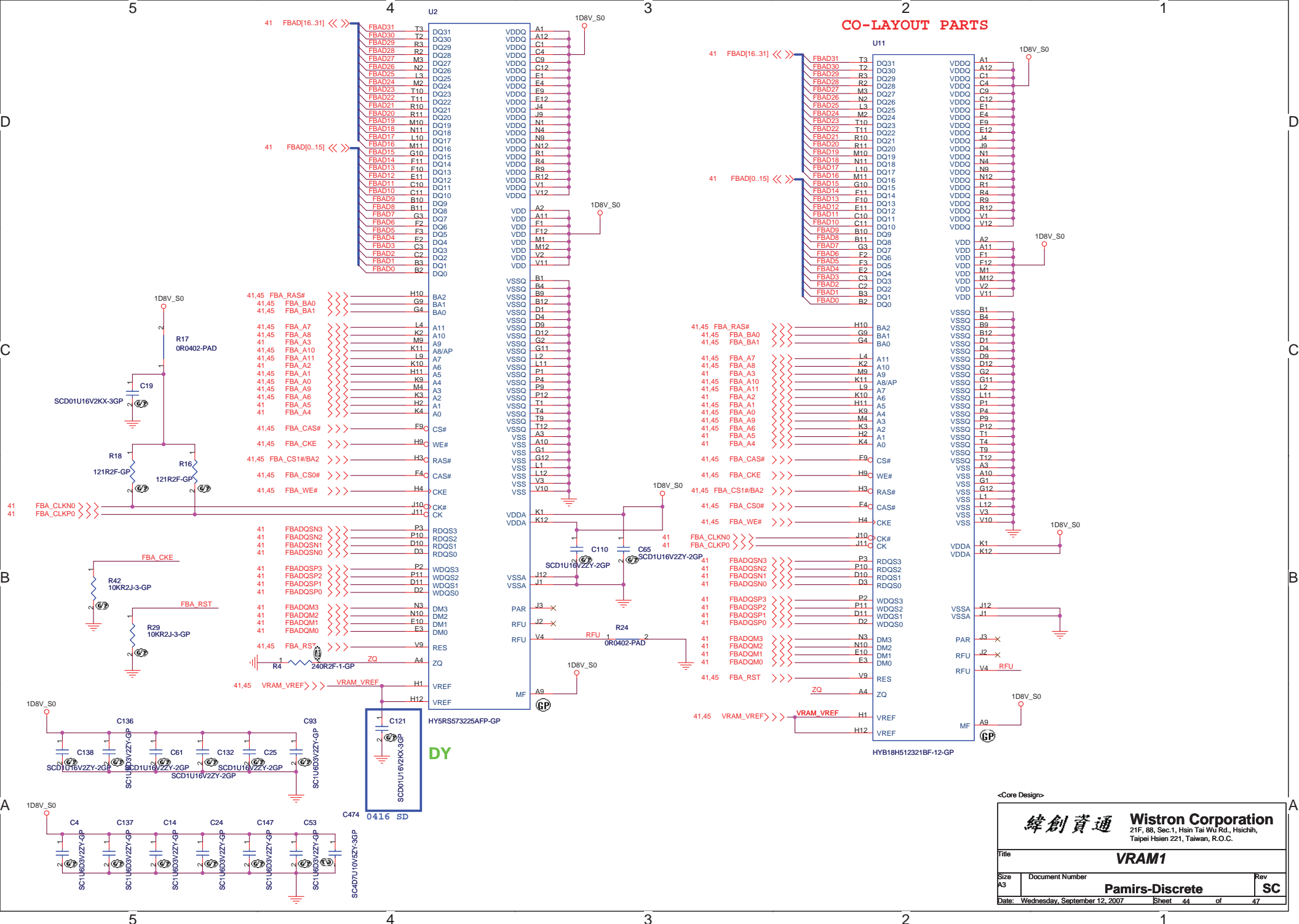
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Title: **NB8M-GS (2 of 3)**

Size: A3	Document Number: Pamirs-Discrete	Rev: SC
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Date: Wednesday, September 12, 2007 Sheet 42 of 47



<Core Design>

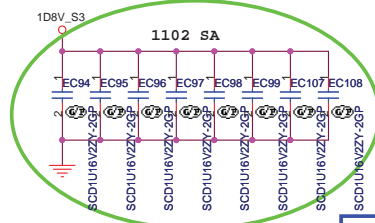
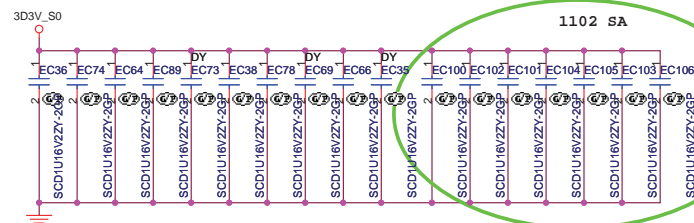
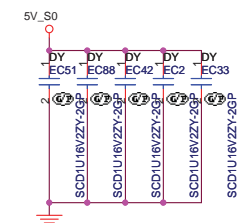
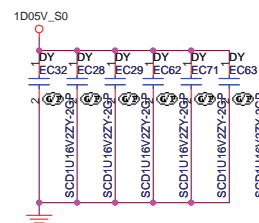
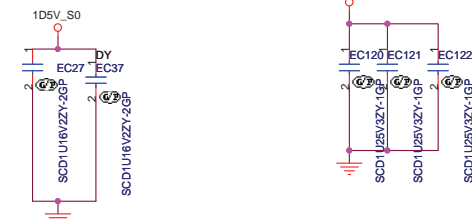
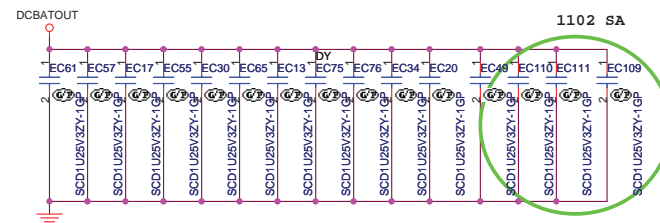
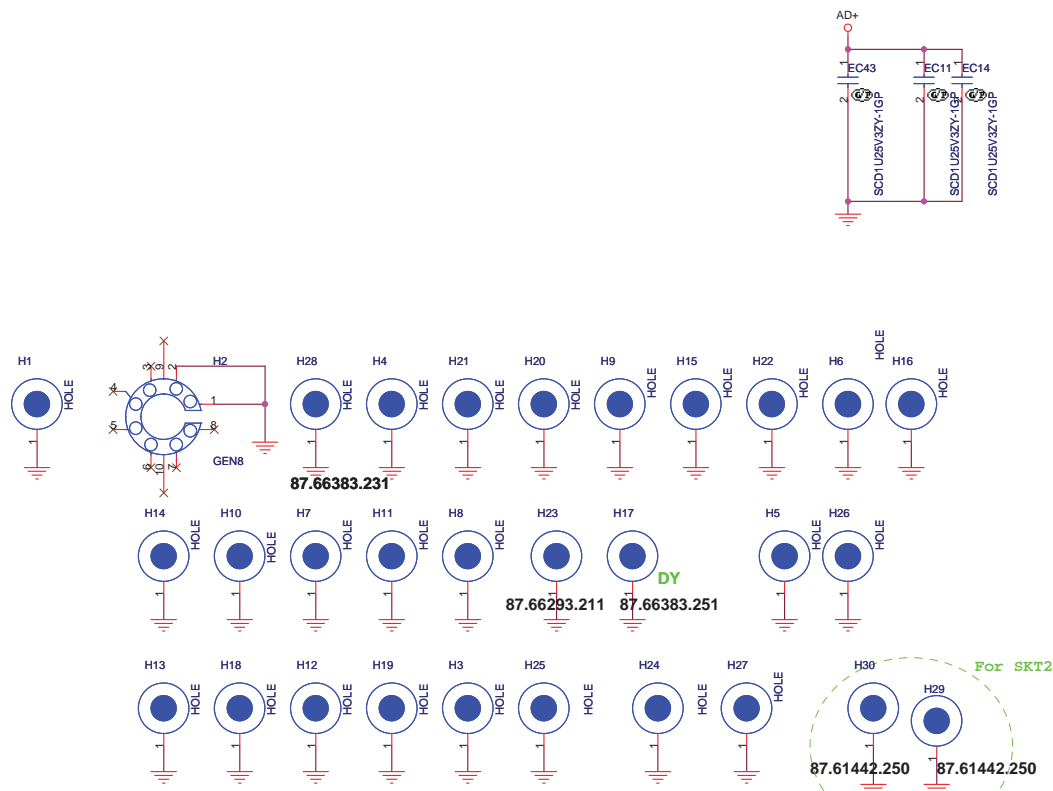
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Title		
VRAM1		
Size A3	Document Number	Rev SC
Date: Wednesday, September 12, 2007		
Sheet 44	of 47	

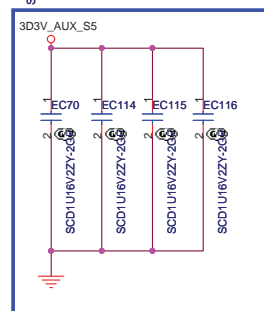
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AD/BATT CONN			
Size	Document Number		Rev
A3		Pamirs-Discrete	SC
Date:	Wednesday, September 12, 2007	Sheet 46 of 47	



0410 SD



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Title	MISC		
Size	Document Number	Pamirs-Discrete	
A3			Rev SC
Date:	Wednesday, September 12, 2007	Sheet 47	of 47